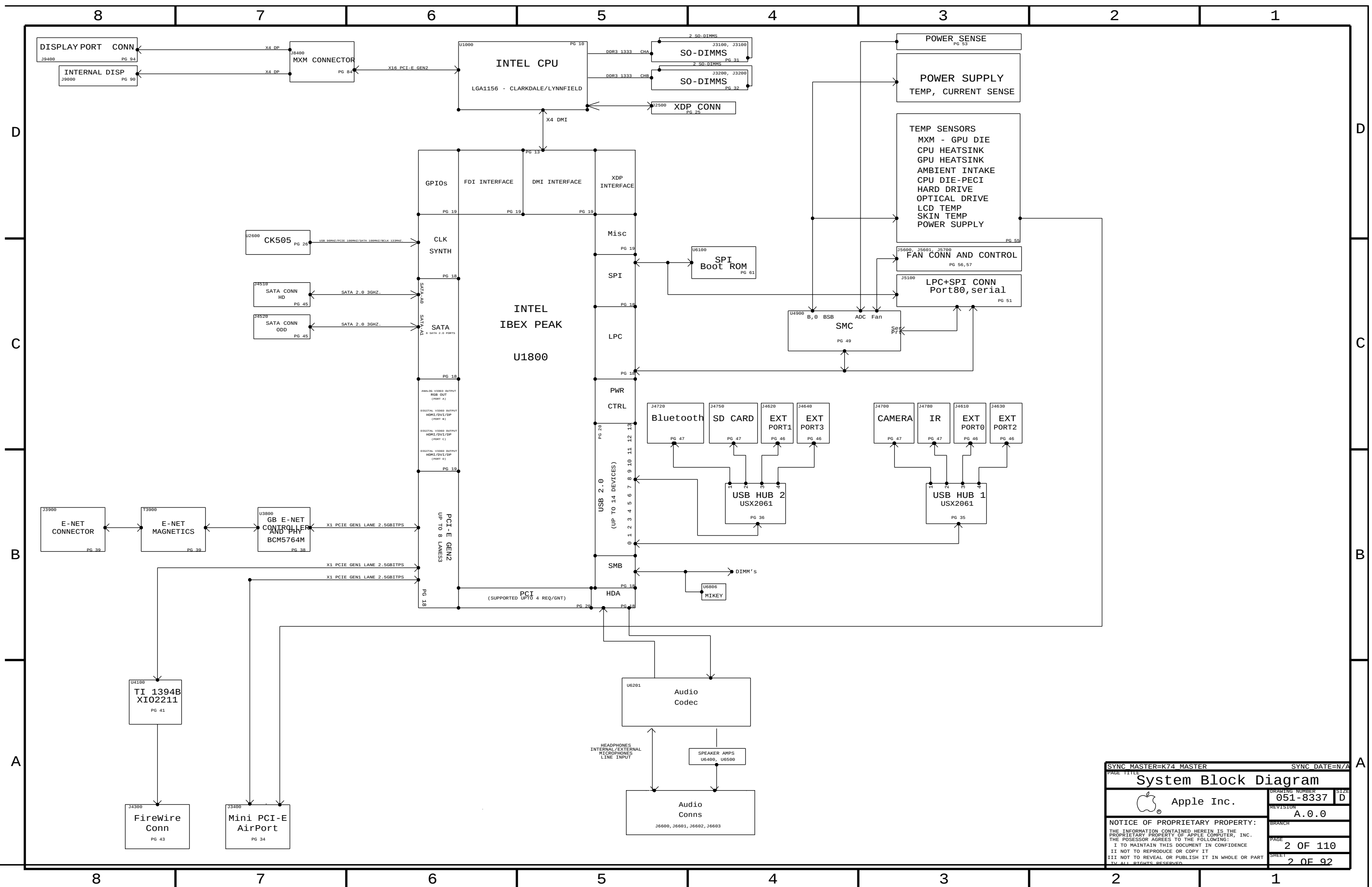




BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-1107	PCBA, MLB, DEV, K74	DEVELOPMENT, DEV_GROUP
639-0698	PCBA, MLB, K74, 2.93GHZ, CKD	K74, 2P93GHZ_CKD_CPU, BASIC, CLARKDALE_73W
639-0707	PCBA, MLB, K74, 3.06GHZ, CKD	K74, 3P06GHZ_CKD_CPU, BASIC, CLARKDALE_73W
639-0808	PCBA, MLB, K74, 3.20GHZ, CKD	K74, 3P20GHZ_CKD_CPU, BASIC, CLARKDALE_73W
639-0695	PCBA, MLB, K74, 3.46GHZ, CKD	K74, 3P46GHZ_CKD_CPU, BASIC, CLARKDALE_73W
639-0991	PCBA, MLB, K74, 3.60GHZ, CKD	K74, 3P60GHZ_CKD_CPU, BASIC, CLARKDALE_73W
639-0694	PCBA, MLB, K74, 2.53GHZ, LFD	K74, 2P53GHZ_LFD_CPU, BASIC, LYNNFIELD_82W

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE, XDP, MXM, XDP_CPU_BPM, PCH_VRM, BUF_CLK, HUB_USX2061, FW_TI_INT_VREG, BCM5764M, SD_USB, METAL_IO, PRODUCTION
DEV_GROUP	XDP_CONN, LPCPLUS, MOJOMUX, CPU_1V5_SENSE, VREFMRGN

CPU SOCKET & ILM SUB-BOMS

ALTERNATE SOCKET VENDORS MUST USE MATCHING ILM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0063	1	SOCKET, LGA1156, CPU- LF	U1000	CRITICAL	MOLEX_SOCKET
604-1161	1	ASSY, PURCHASED, ILM, MOLEX, K74	ILM	CRITICAL	MOLEX_SOCKET
511S0069	1	SOCKET, LGA1156, CPU- LF	U1000	CRITICAL	FOXCONN_SOCKET
604-1246	1	ASSY, PURCHASED, ILM, MOLEX, K74	ILM	CRITICAL	FOXCONN_SOCKET

BOM NUMBER	BOM NAME	BOM OPTIONS
607-6694	SUB ASSY,CPU SOCKET,K74,MOLEX	MOLEX_SOCKET
607-6693	SUB ASSY,CPU SOCKET,K74,FOXCONN	FOXCONN_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
607-6694	1	MOLEX CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
607-6693	607-6694		SKT_ILM	FOXCONN ALTERNATE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3828	1	IC, I2C, PEAK PRQ, DESKTOP, FCGBA, PCH, P425	U1800	CRITICAL	
359S0157	1	IC, SLG2AP108, CLK GEN, CK505, QFN3	U2600	CRITICAL	BUF_CLK
341T0230	1	IC, EFI BOOTROM, K74/K75	U6100	CRITICAL	
338S0765	1	IC, X102211ZAY, 1394B_PCIE, PHY/LINK	U4100	CRITICAL	
825-7122	1	MLB LABEL, 48.0X4.8	X14	CRITICAL	
343S0493	1	IC, BCM5764M, ENET, 8X8	U3900	CRITICAL	BCM5764M
343S0494	1	IC, BCM57765A, ENET&SD, 8X8	U3900	CRITICAL	BCM57765
341T0269	1	ENET 1MBIT FLASH, CII, K74/K75	U3990	CRITICAL	BCM5764M
341T0246	1	ENET 1MBIT FLASH, CIV, K74/K75	U3990	CRITICAL	BCM57765

RAW: 335S0663

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3837	1	CKD, Q3GR, QS, 2.93, 73M, 1333, C2, 4M, LGA	CPU	CRITICAL	2P93GHZ_CKD_CPU
337S3912	1	CKD, SLBTD, PRQ, 3.06, 73M, 1333, K0, 4M, LGA	CPU	CRITICAL	3P06GHZ_CKD_CPU
337S3911	1	CKD, SLBUD, PRQ, 3.20, 73M, 1333, K0, 4M, LGA	CPU	CRITICAL	3P20GHZ_CKD_CPU
337S3900	1	CKD, SLBLT, PRQ, 3.46, 73M, 1333, C2, 4M, LGA	CPU	CRITICAL	3P46GHZ_CKD_CPU
337S3910	1	CKD, SLBTH, PRQ, 3.60, 73M, 1333, K0, 4M, LGA	CPU	CRITICAL	3P60GHZ_CKD_CPU
337S3862	1	LFD, Q3C6, QS, 2.53, 82W, 1333, B1, 8M, LGA	CPU	CRITICAL	2P53GHZ_LFD_CPU

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3898	337S3912	3P06GHZ_CKD_CPU		C2, PRQ, 3.06 GHZ CKD

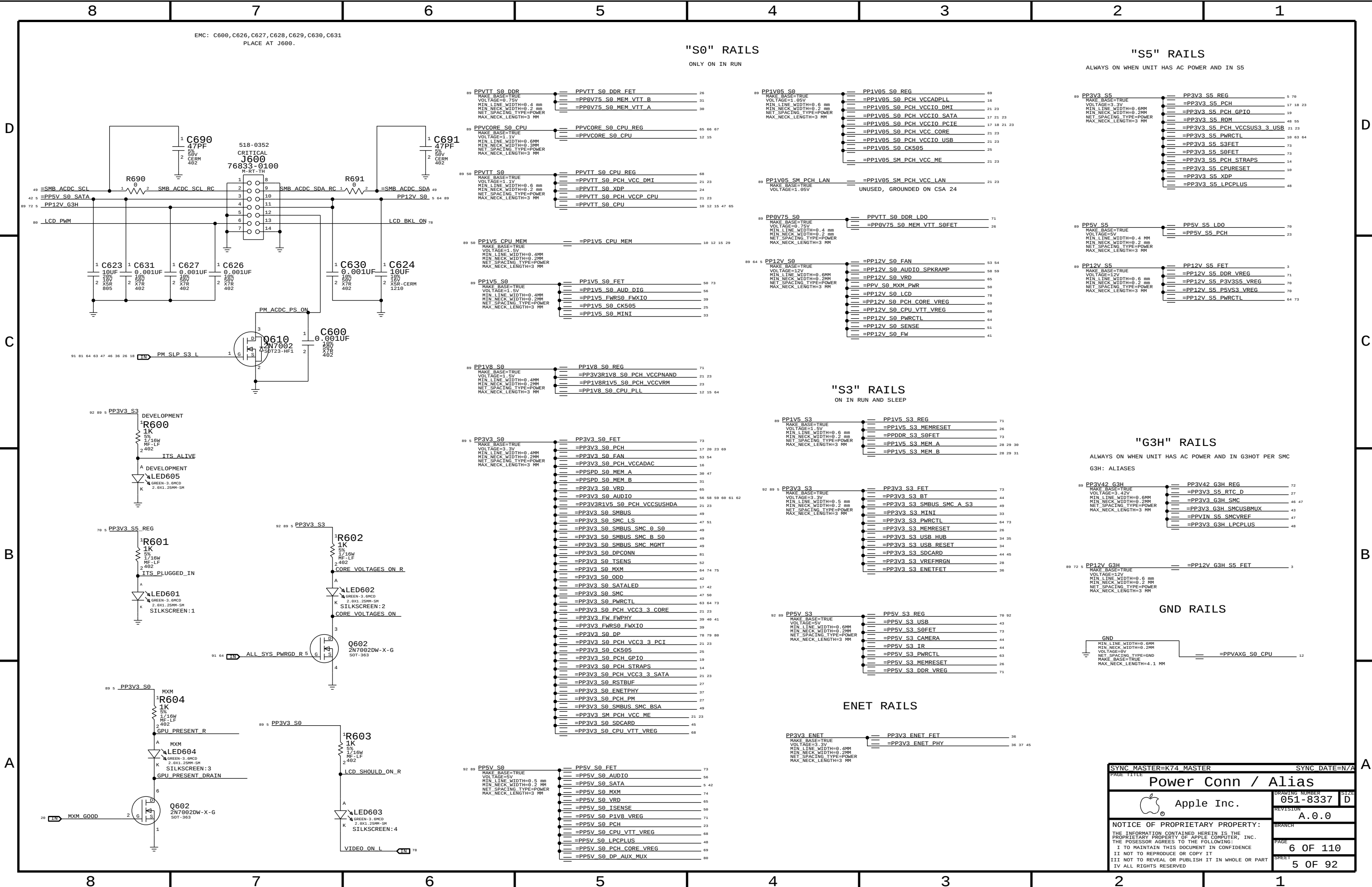
K74 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8337	1	SCH, MLB, K74	SCH1		
820-2784	1	PCBF, MLB, K74	MLB1		
341T0231	1	IC, SMC, K74	U4900	CRITICAL	K74

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0339	197S0179		Y4190	FIREWIRE OSCILLATOR
128S0298	128S0293		C1670, C7260, C7444	

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BOM Configuration			
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EMC: C600, C626, C627, C628, C629, C630, C631
PLACE AT J600.

"S0" RAILS

ONLY ON IN RUN

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

"S3" RAILS

ON IN RUN AND SLEEP

"G3H" RAILS

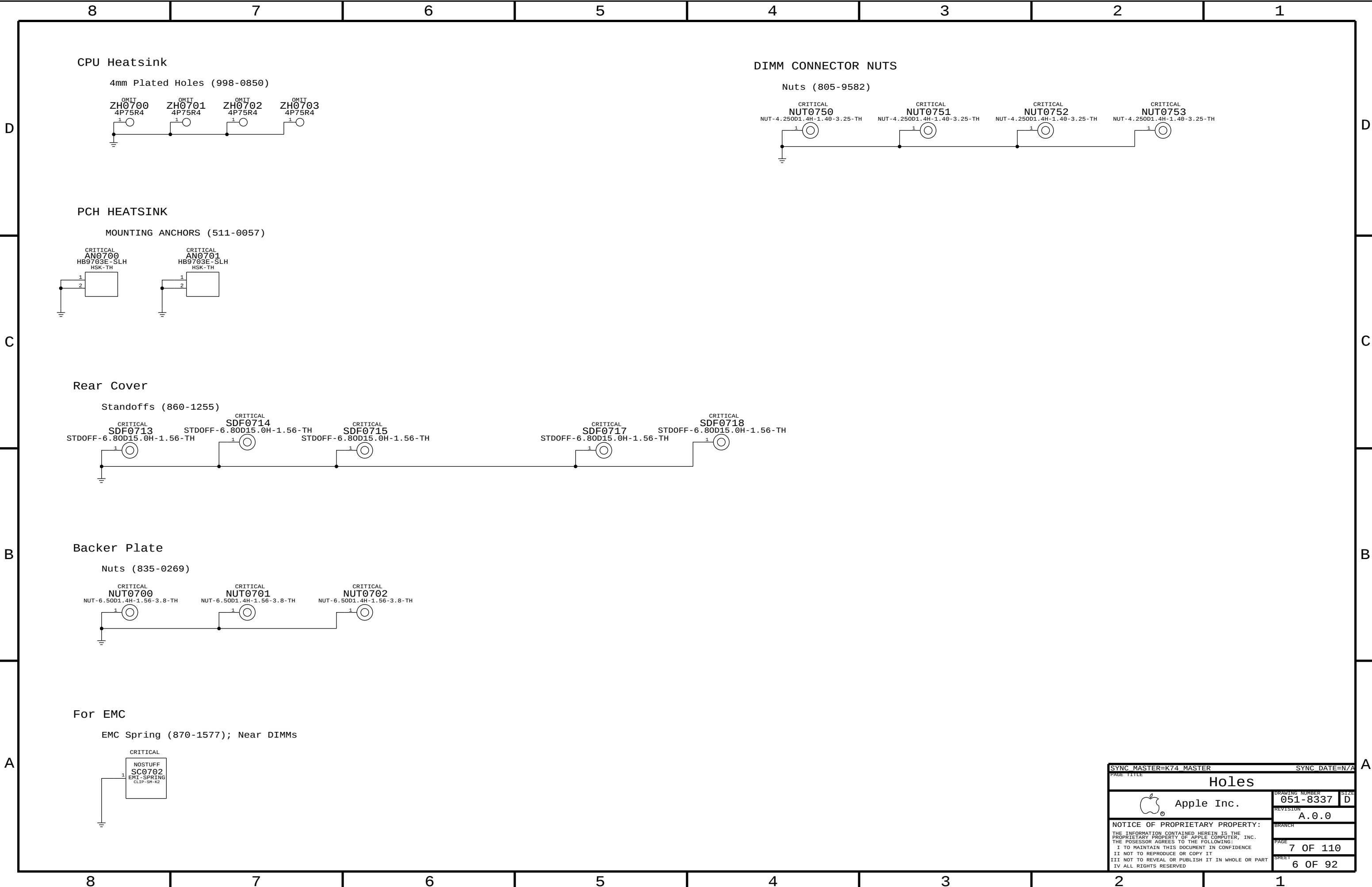
ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

G3H: ALIASES

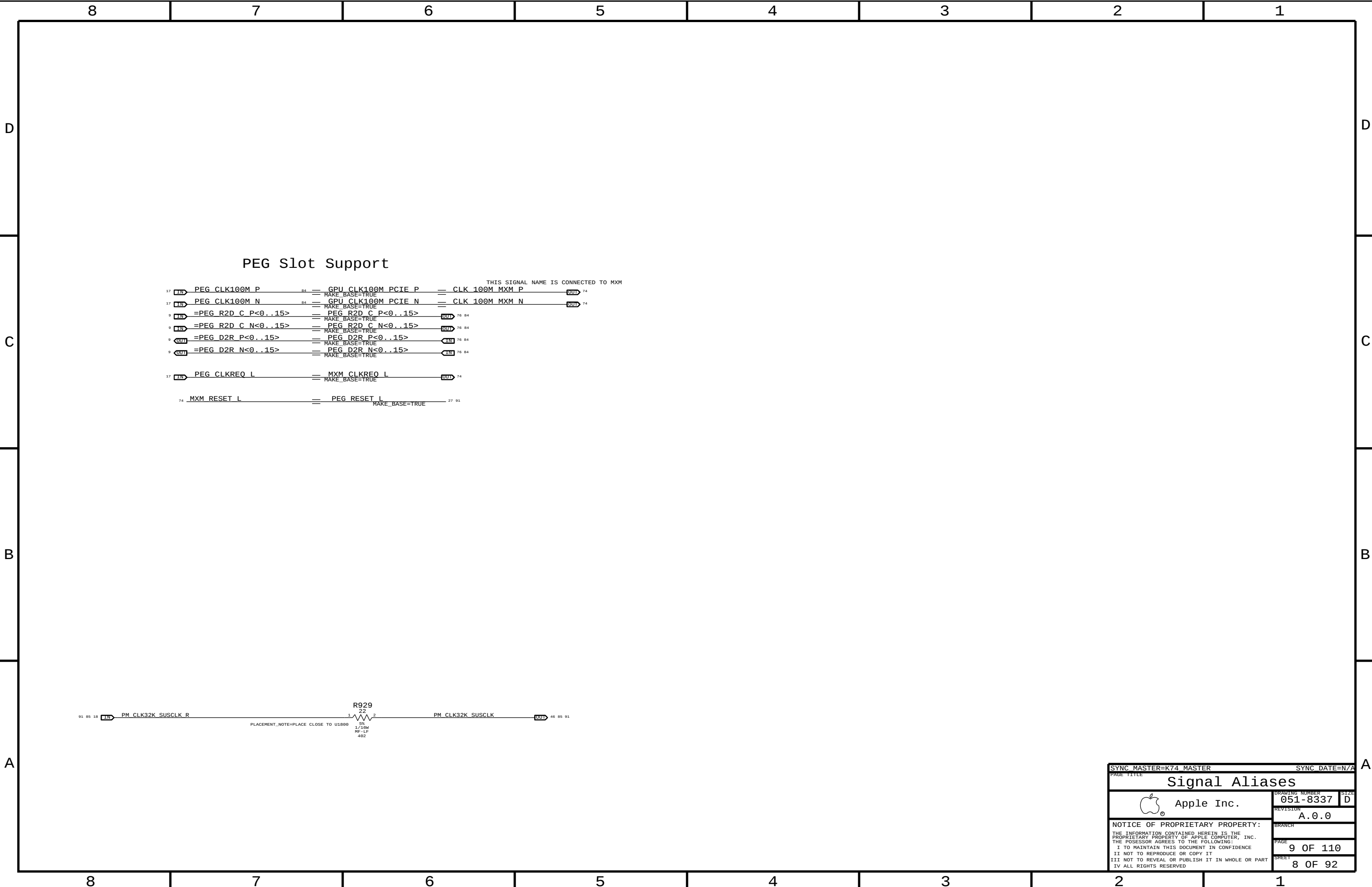
GND RAILS

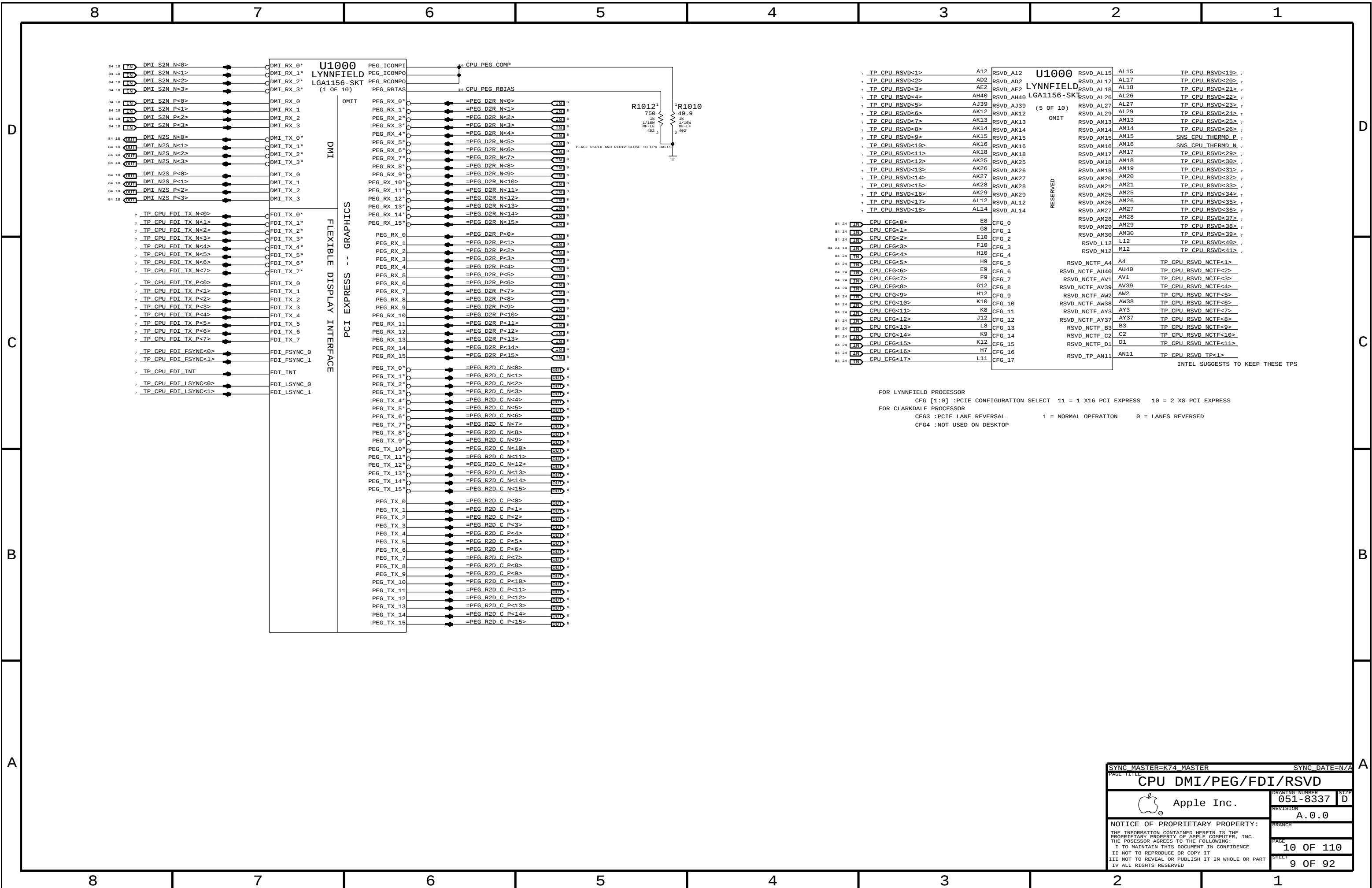
ENET RAILS

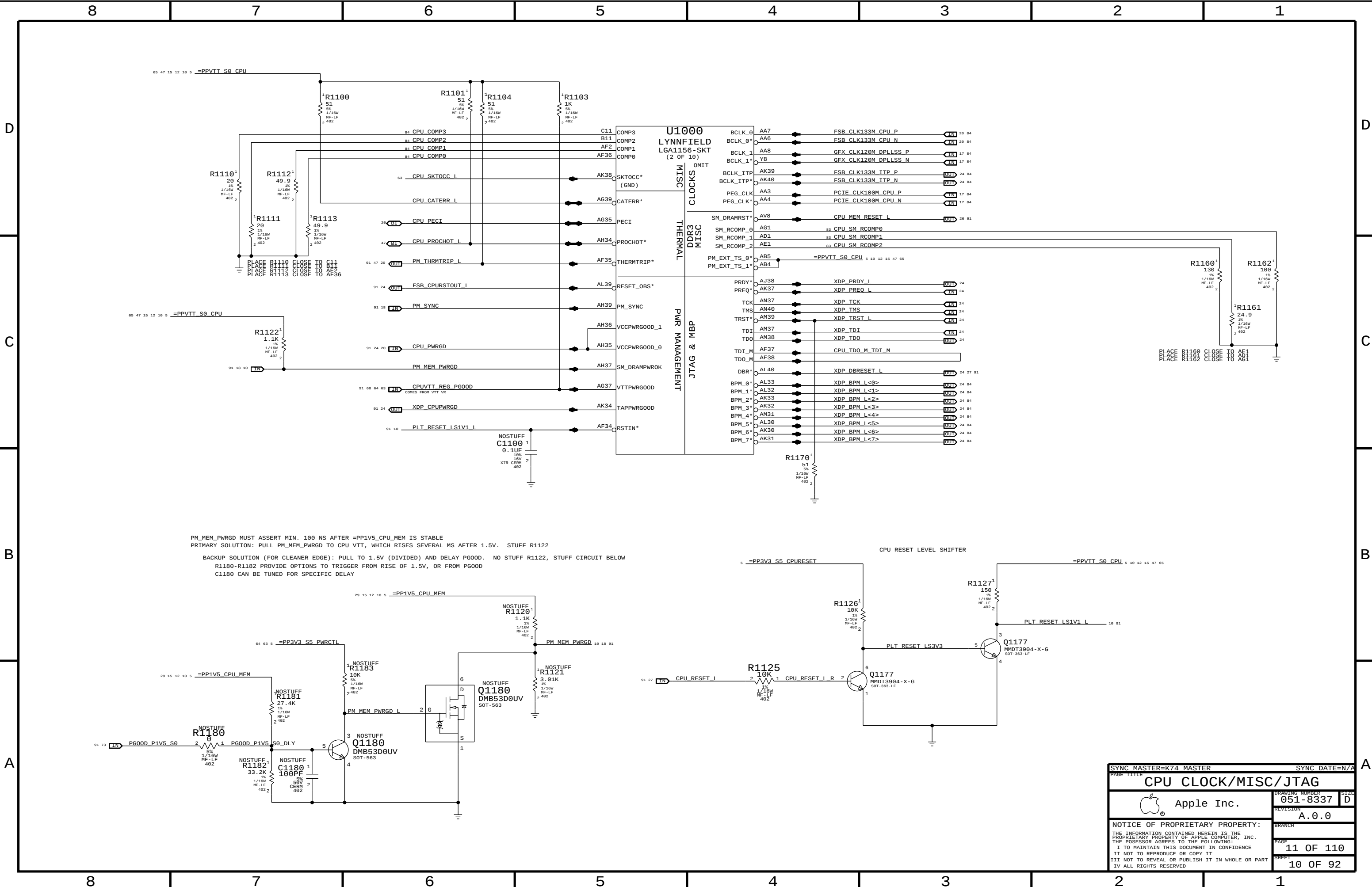
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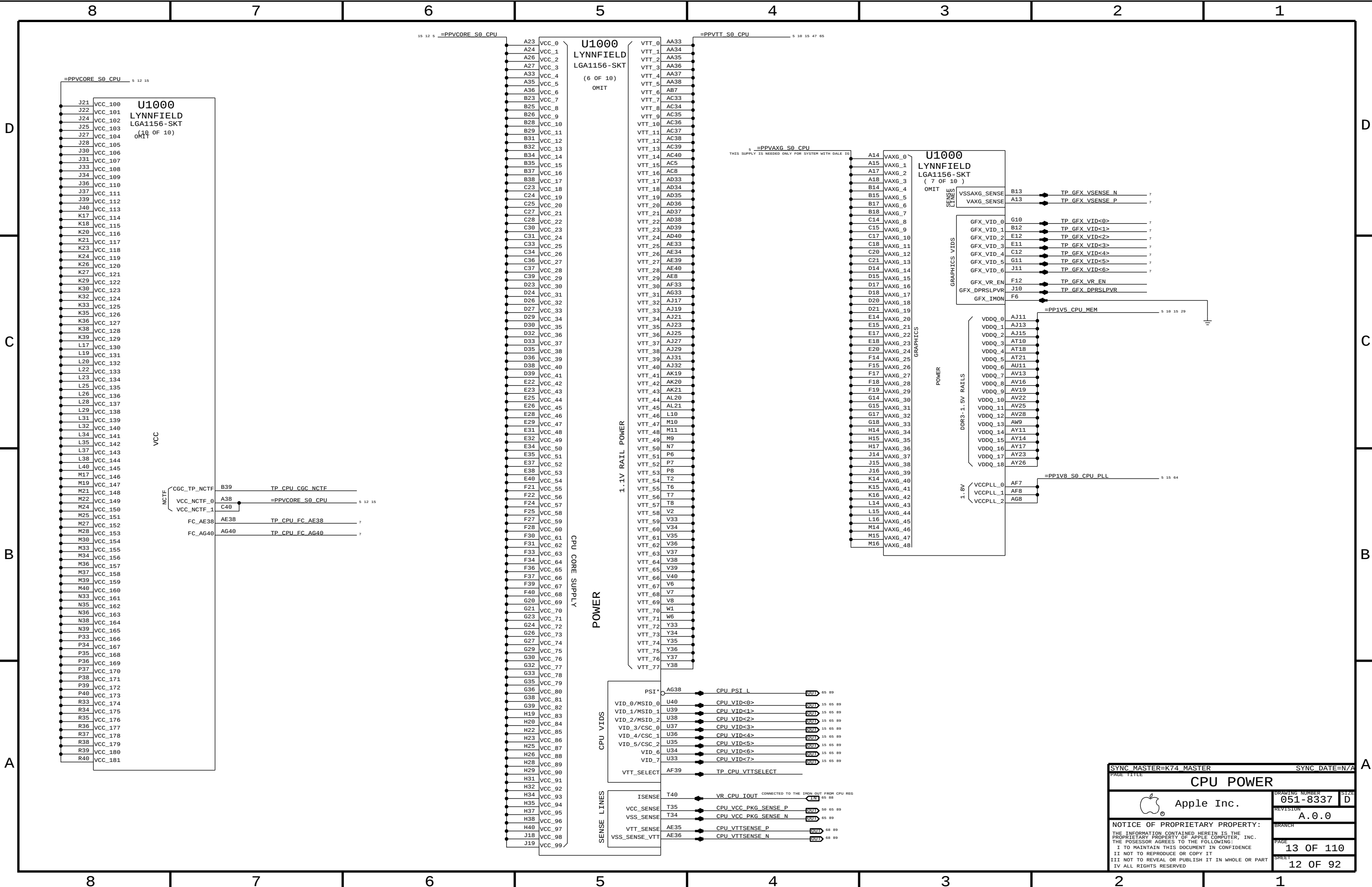


PM_MEM_PWRGD MUST ASSERT MIN. 100 NS AFTER =PP1V5_CPU_MEM IS STABLE
PRIMARY SOLUTION: PULL PM_MEM_PWRGD TO CPU VTT, WHICH RISES SEVERAL MS AFTER 1.5V. STUFF R1122

BACKUP SOLUTION (FOR CLEANER EDGE): PULL TO 1.5V (DIVIDED) AND DELAY PG00D. NO-STUFF R1122, STUFF CIRCUIT BELOW
R1180-R1182 PROVIDE OPTIONS TO TRIGGER FROM RISE OF 1.5V, OR FROM PG00D
C1180 CAN BE TUNED FOR SPECIFIC DELAY

CPU RESET LEVEL SHIFTER

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CPU CLOCK/MISC/JTAG		DRAWING NUMBER	SIZE
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CPU POWER

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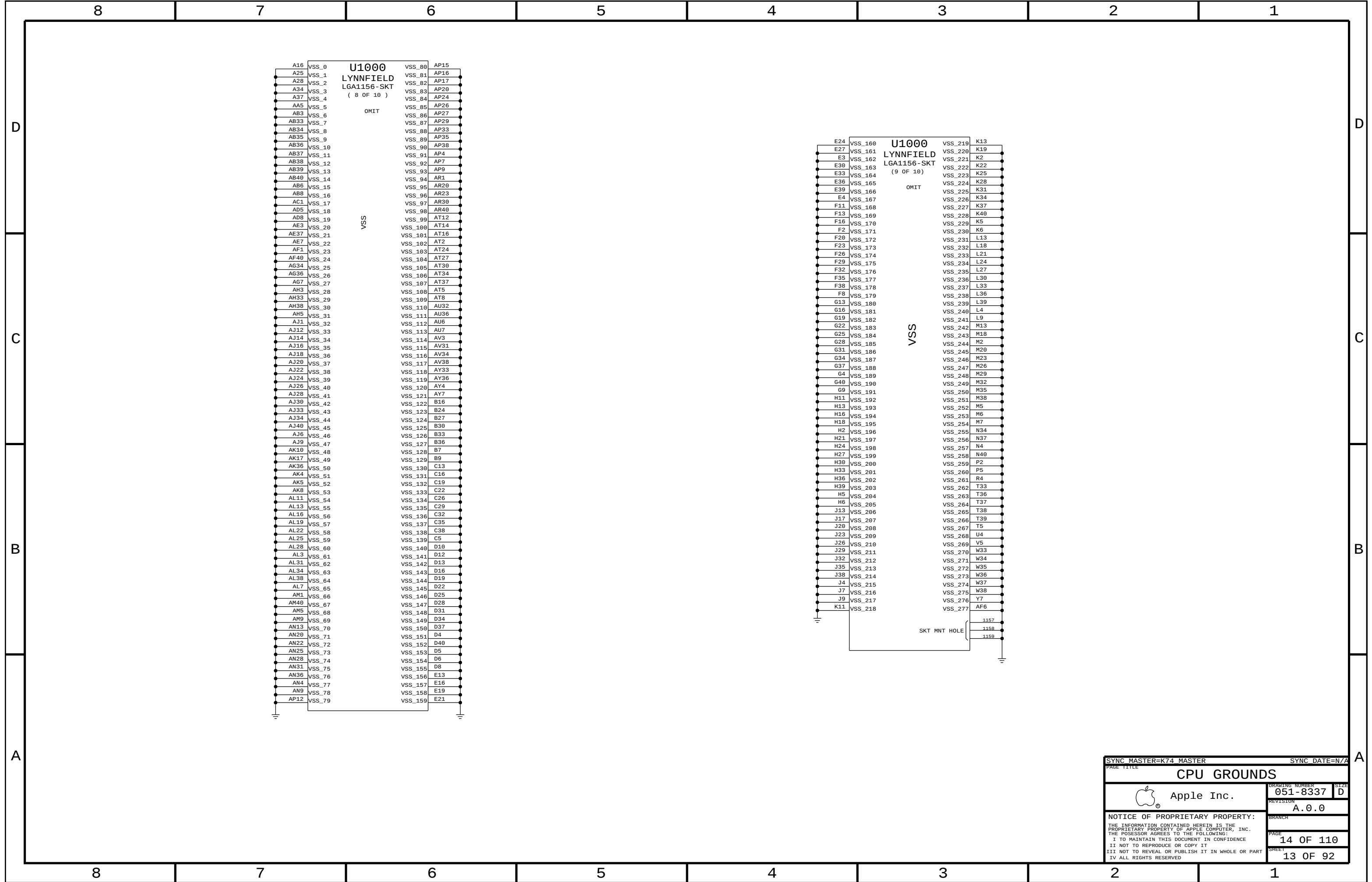
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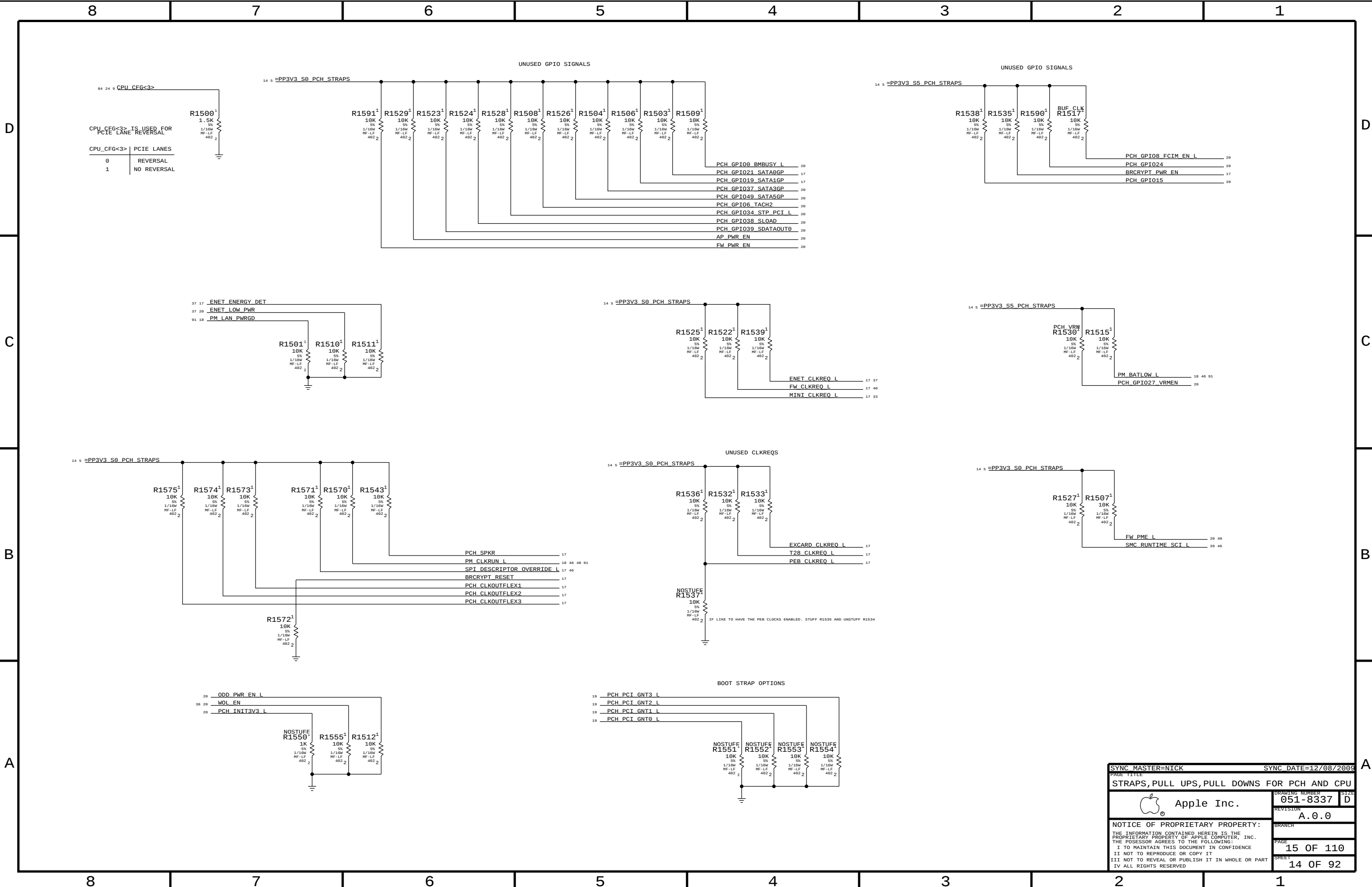
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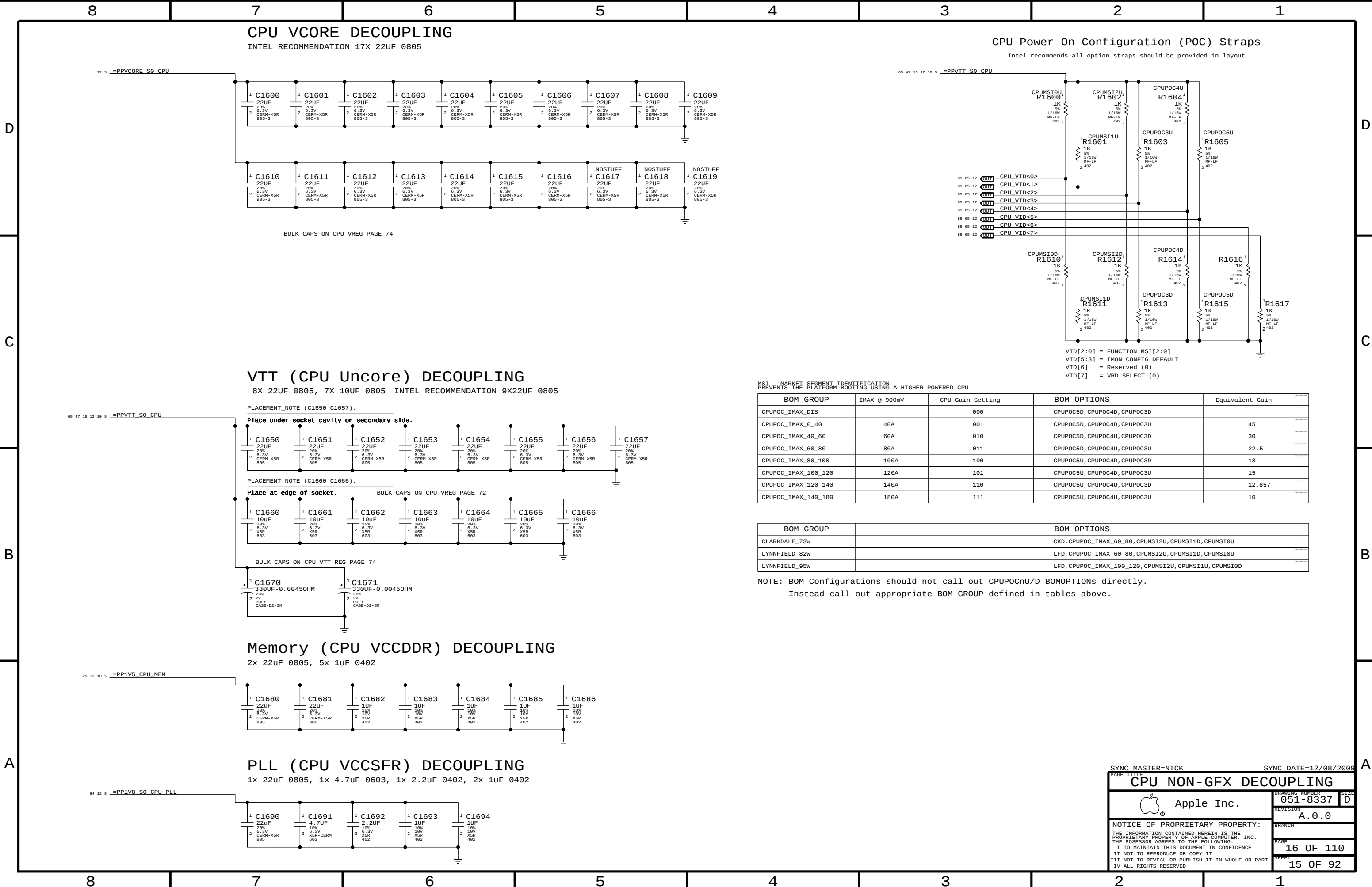
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CPU Vcore DECOUPLING

INTEL RECOMMENDATION 17X 22UF 0805

CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout

VTT (CPU Uncore) DECOUPLING

8X 22UF 0805, 7X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805

Memory (CPU VCCDDR) DECOUPLING

2x 22uF 0805, 5x 1uF 0402

PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402

MSI - MARKET SEGMENT IDENTIFICATION
PREVENTS THE PLATFORM BOOTING USING A HIGHER POWERED CPU

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC5D, CPUPOC4D, CPUPOC3D	
CPUPOC_IMAX_0_40	40A	001	CPUPOC5D, CPUPOC4D, CPUPOC3U	45
CPUPOC_IMAX_40_60	60A	010	CPUPOC5D, CPUPOC4U, CPUPOC3D	30
CPUPOC_IMAX_60_80	80A	011	CPUPOC5D, CPUPOC4U, CPUPOC3U	22.5
CPUPOC_IMAX_80_100	100A	100	CPUPOC5U, CPUPOC4D, CPUPOC3D	18
CPUPOC_IMAX_100_120	120A	101	CPUPOC5U, CPUPOC4D, CPUPOC3U	15
CPUPOC_IMAX_120_140	140A	110	CPUPOC5U, CPUPOC4U, CPUPOC3D	12.857
CPUPOC_IMAX_140_180	180A	111	CPUPOC5U, CPUPOC4U, CPUPOC3U	10

BOM GROUP	BOM OPTIONS
CLARKDALE_73W	CKD, CPUPOC_IMAX_60_80, CPUMSI2U, CPUMSI1D, CPUMSI0U
LYNNFIELD_82W	LFD, CPUPOC_IMAX_60_80, CPUMSI2U, CPUMSI1D, CPUMSI0U
LYNNFIELD_95W	LFD, CPUPOC_IMAX_100_120, CPUMSI2U, CPUMSI1U, CPUMSI0D

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONS directly.
Instead call out appropriate BOM GROUP defined in tables above.

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SYNC DATE=12/08/2009

CPU NON-GFX DECOUPLING

 Apple Inc.

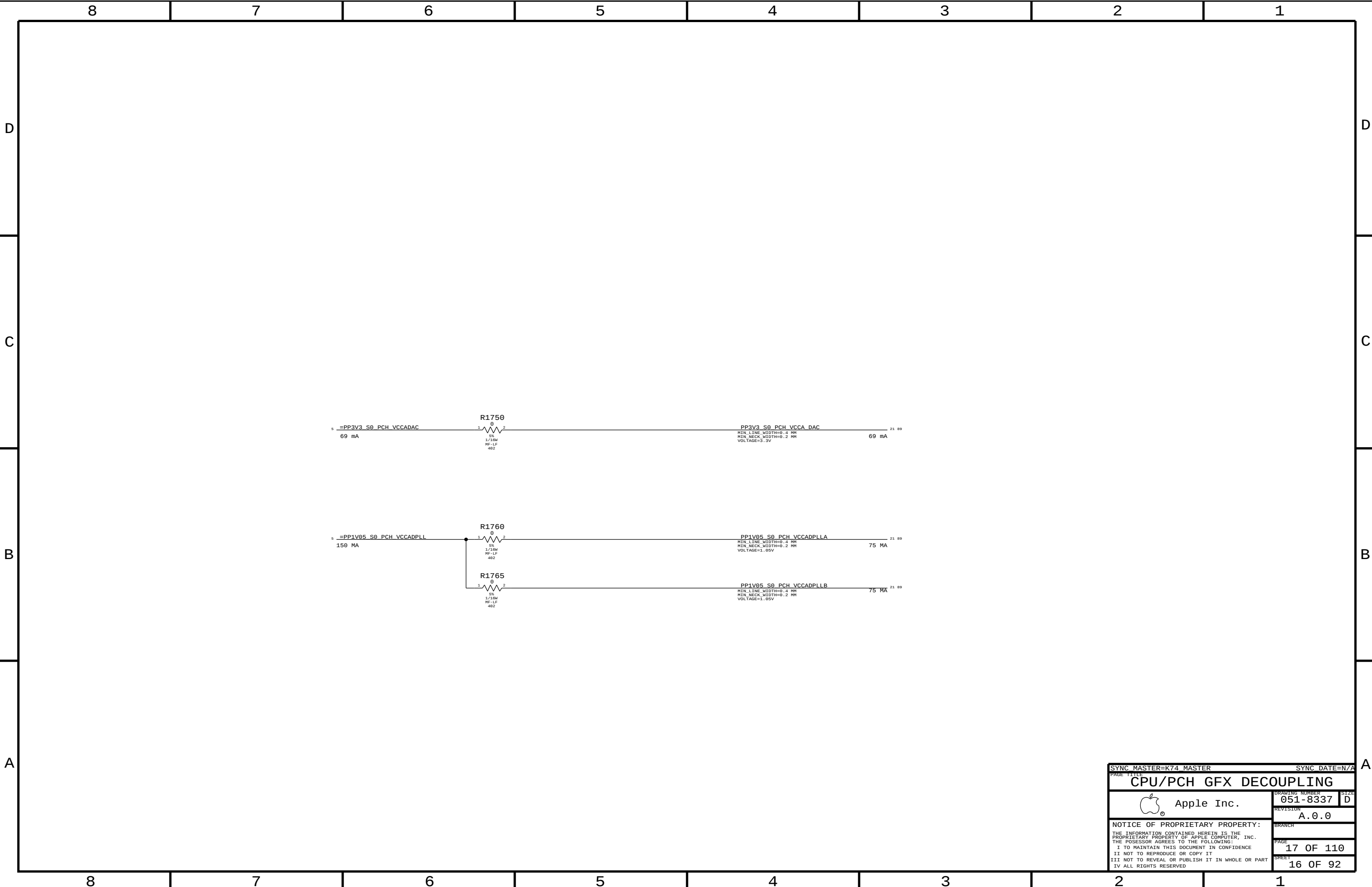
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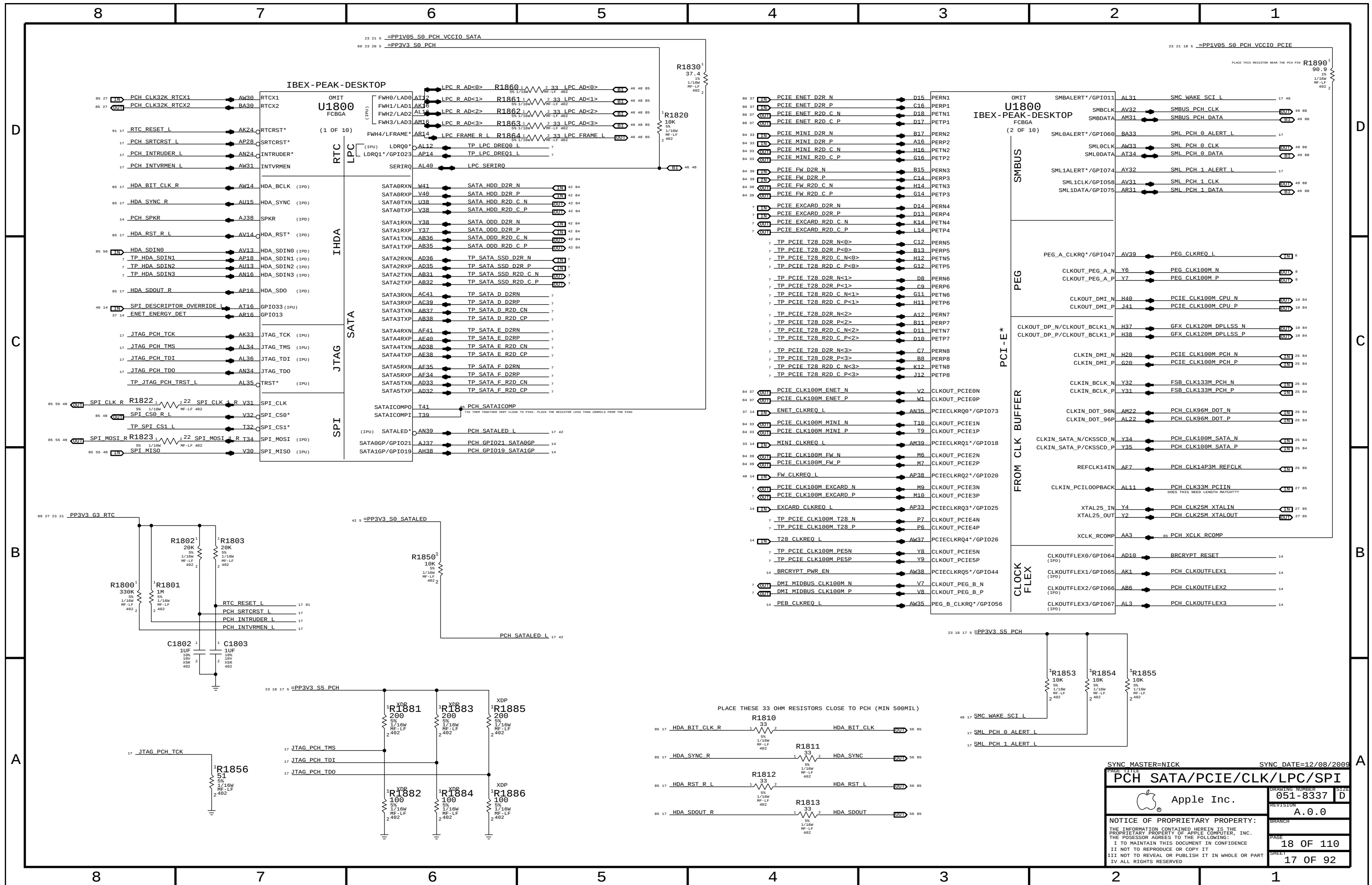
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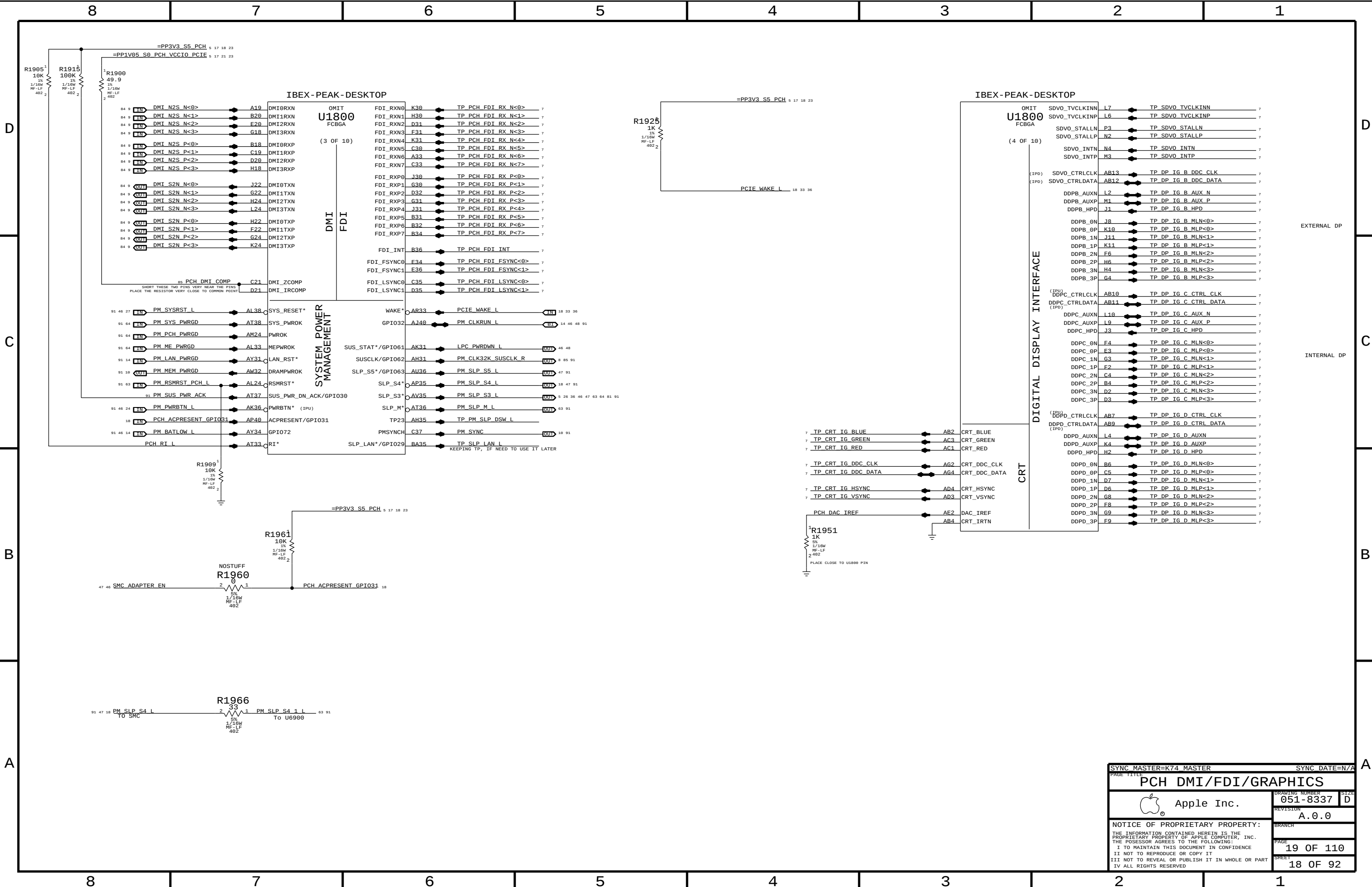
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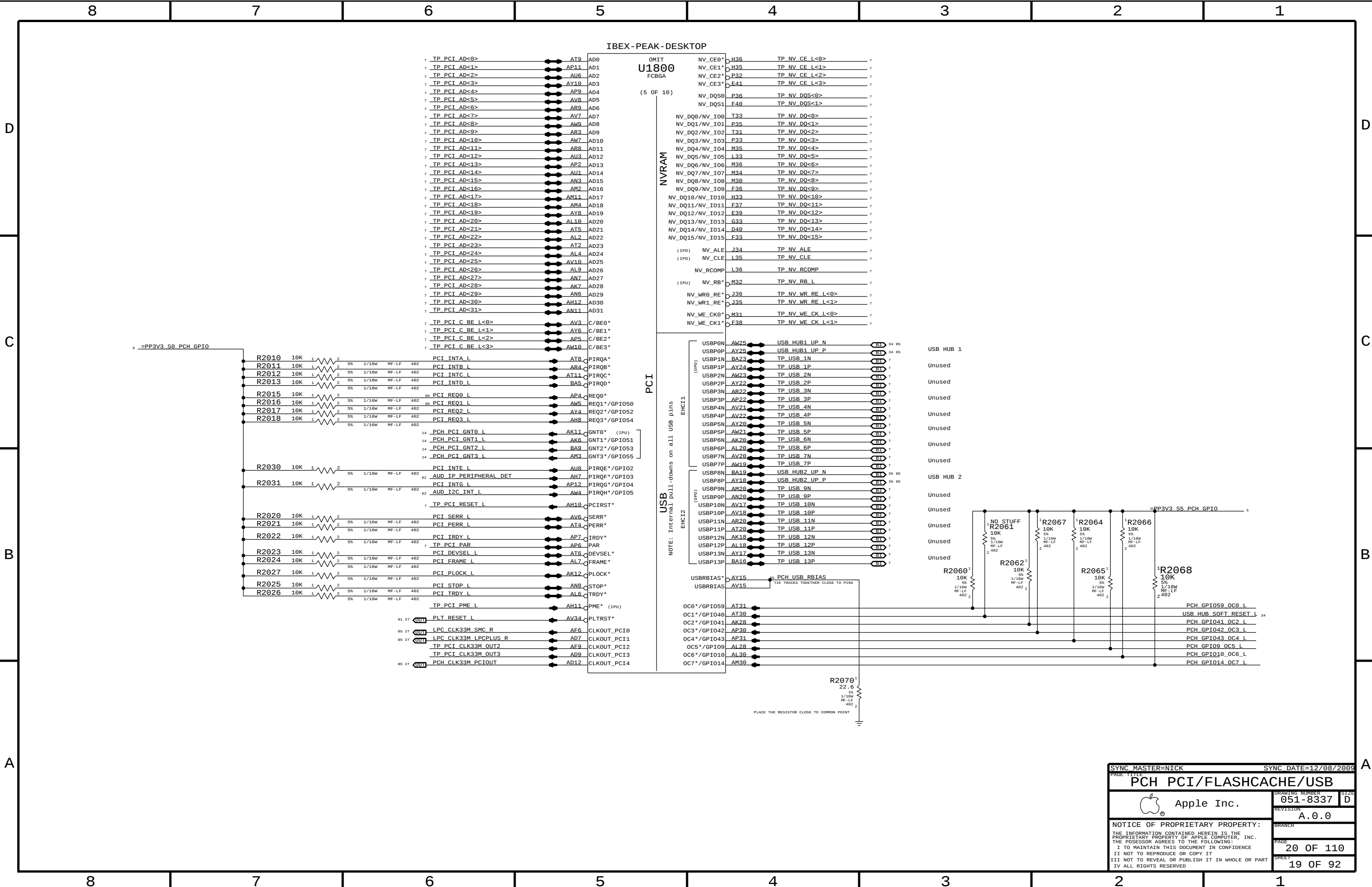
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SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
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CPU/PCH GFX DECOUPLING			
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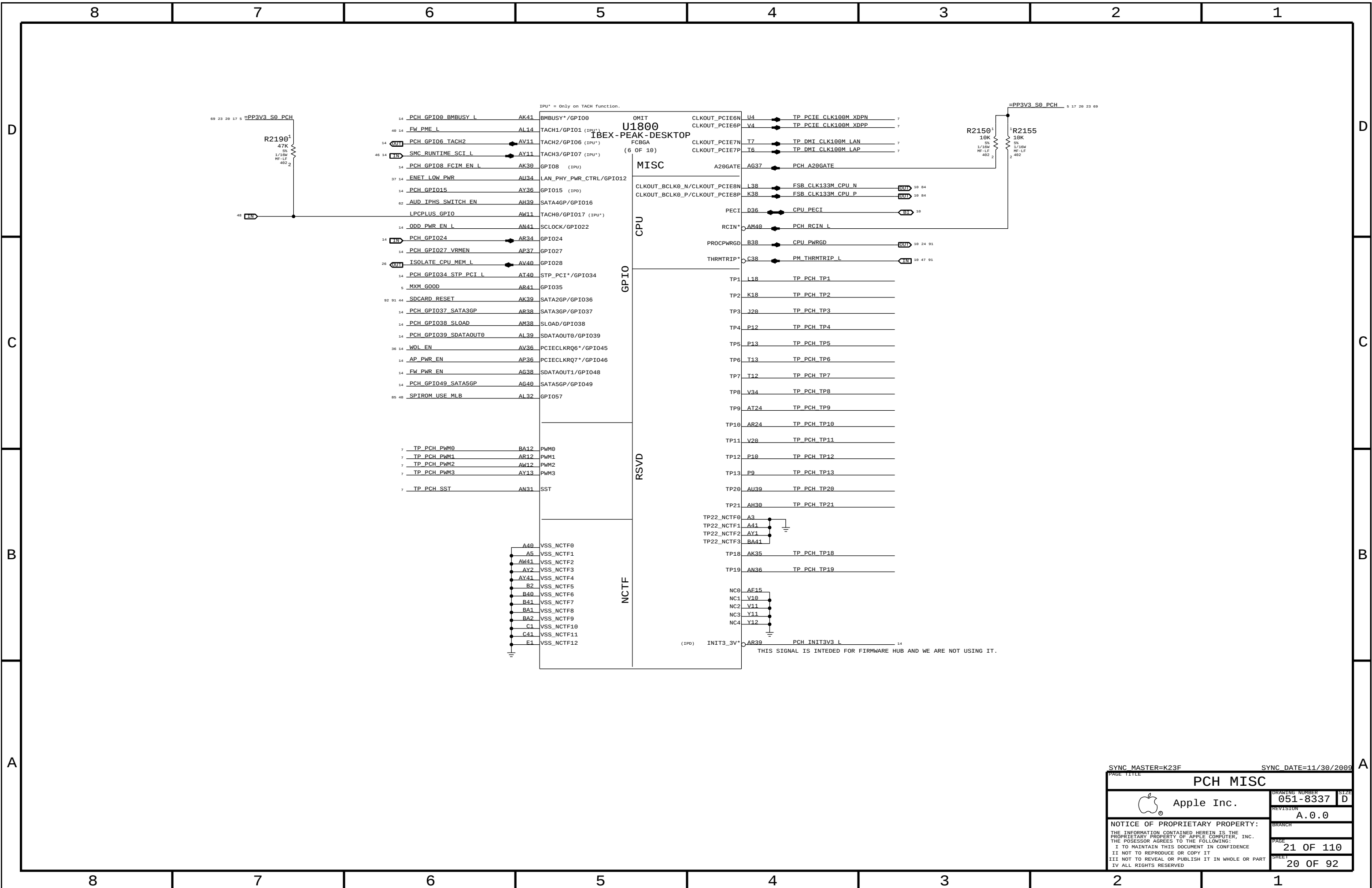


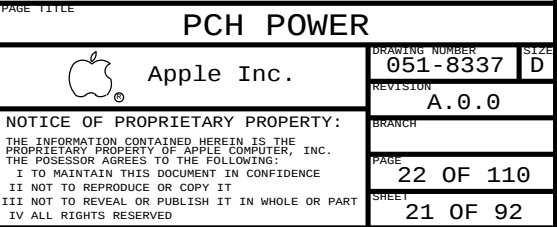


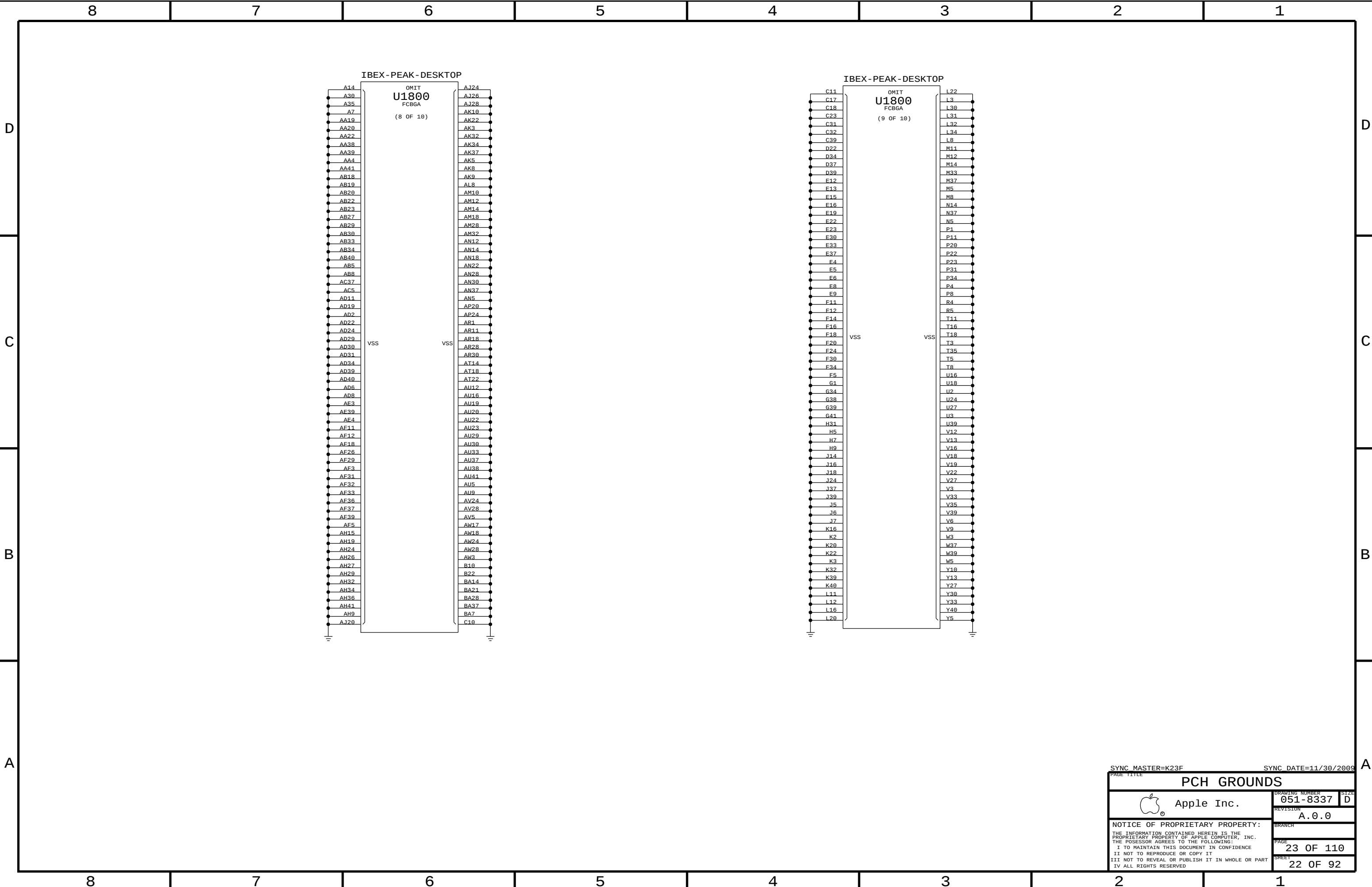


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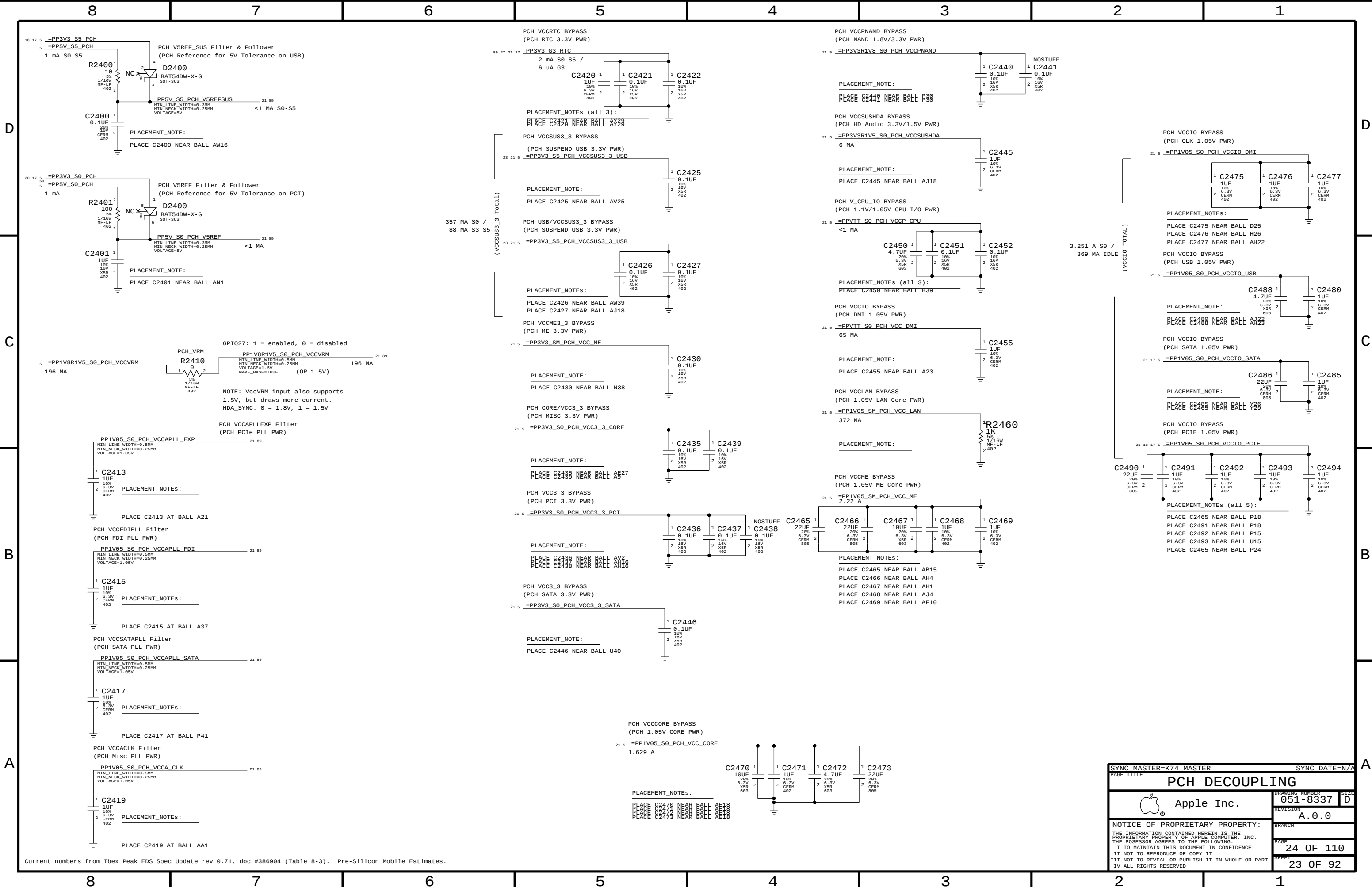




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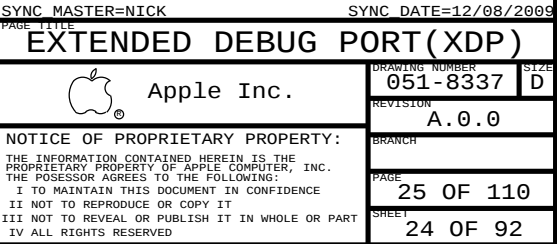
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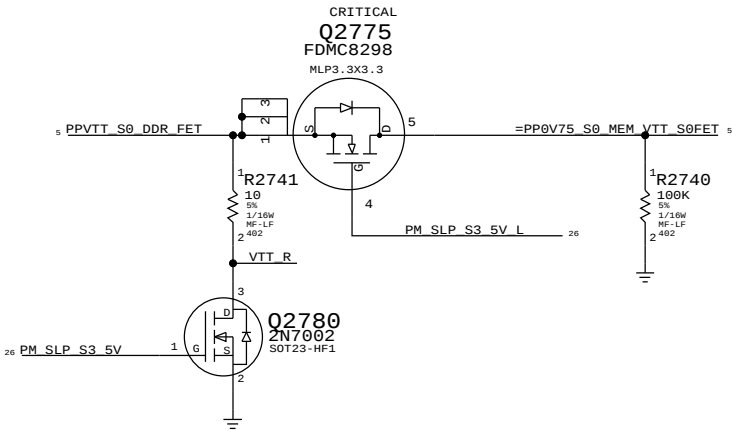
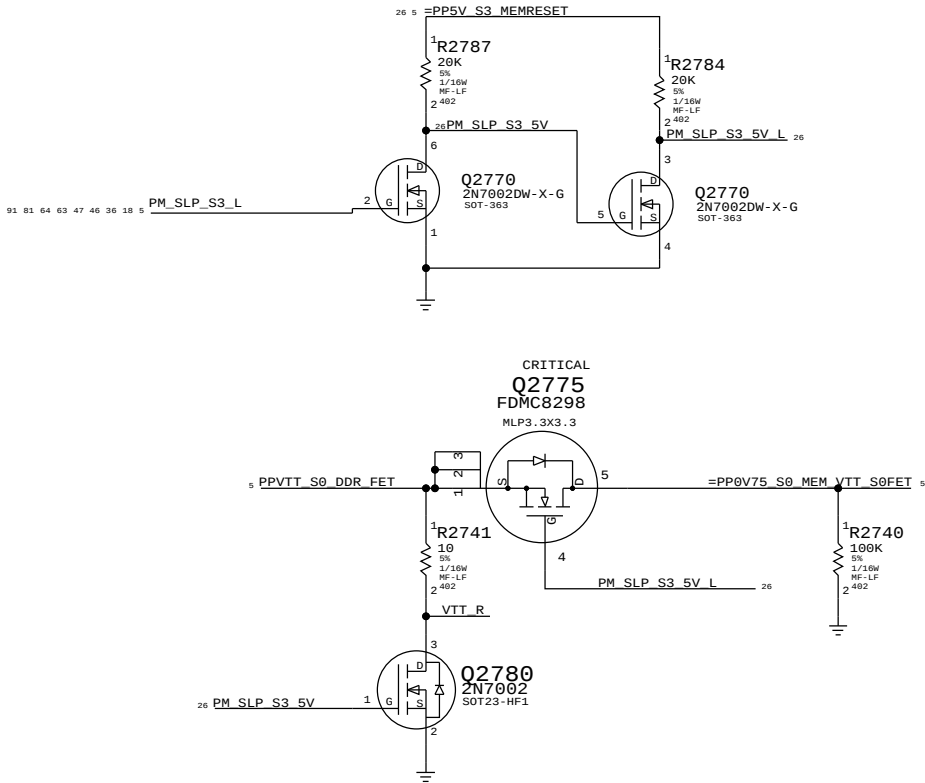
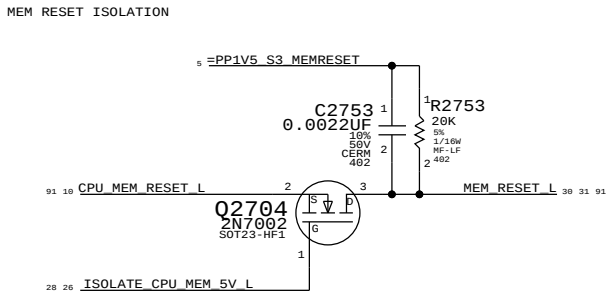
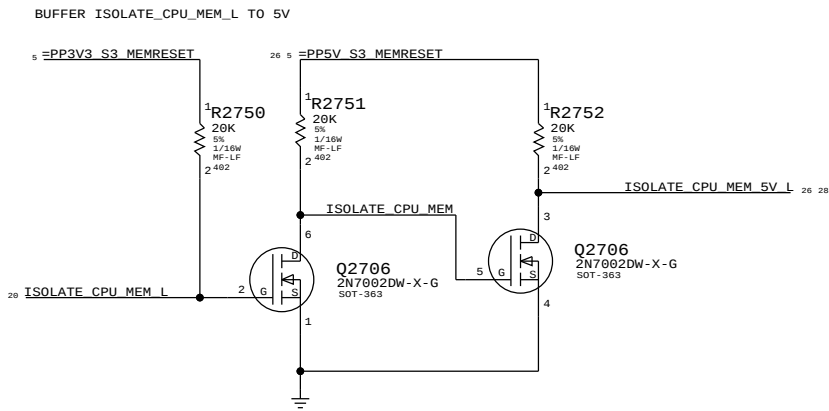
Current numbers from Ixex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

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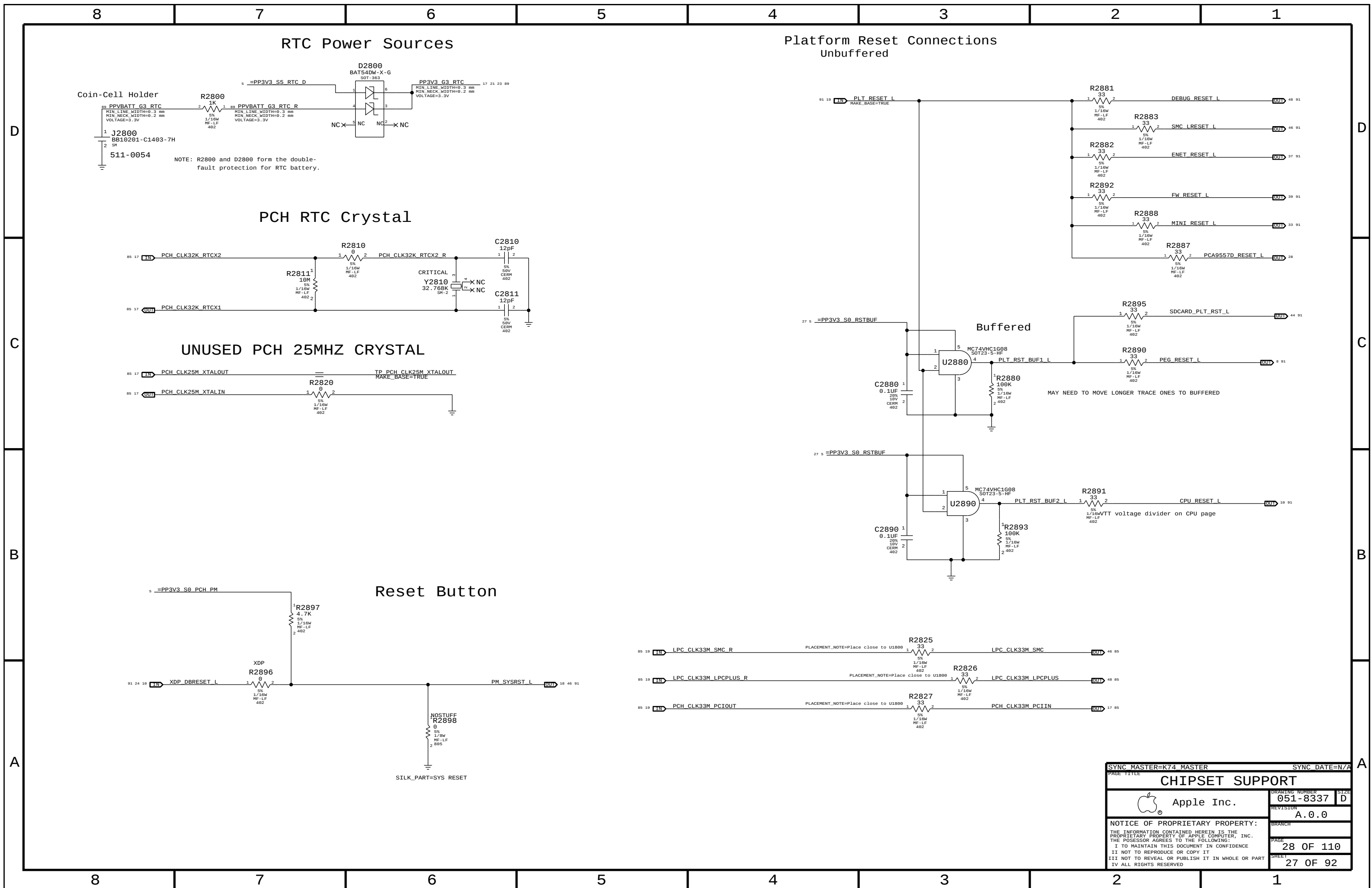


DDR3 RESET Support

LFD CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.



	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0



Page Notes

Power aliases required by this page:

- =PP3V3_S3_VREFMRGN

Signal aliases required by this page:

- =I2C_VREFDACS_SCL

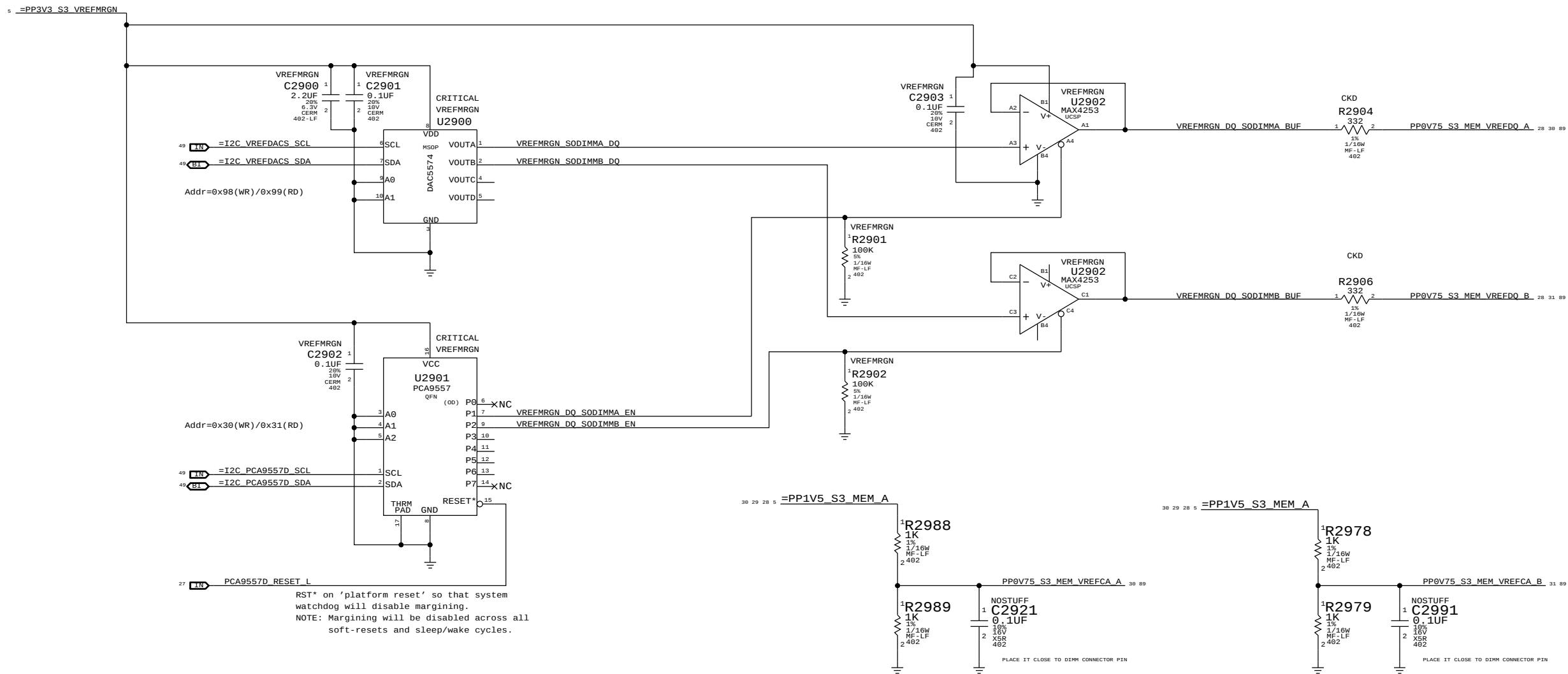
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- =I2C_PCA9557D_SCL

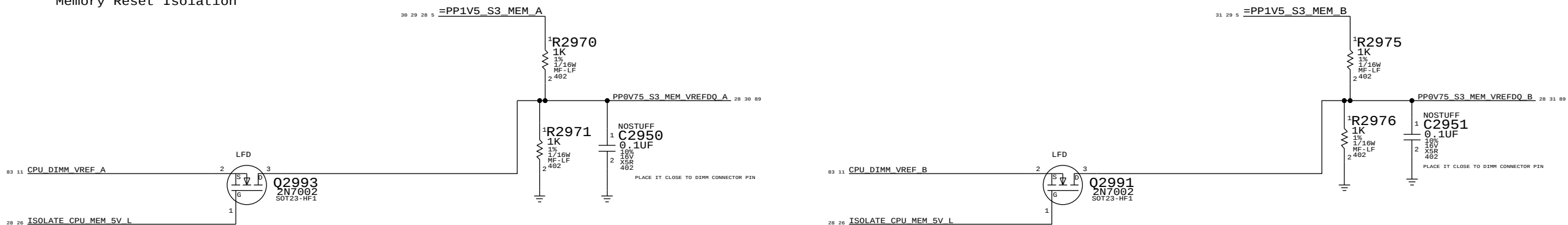
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BOM options provided by this page:

VREFMRGN - Stuffs VREF Margining Circuitry.

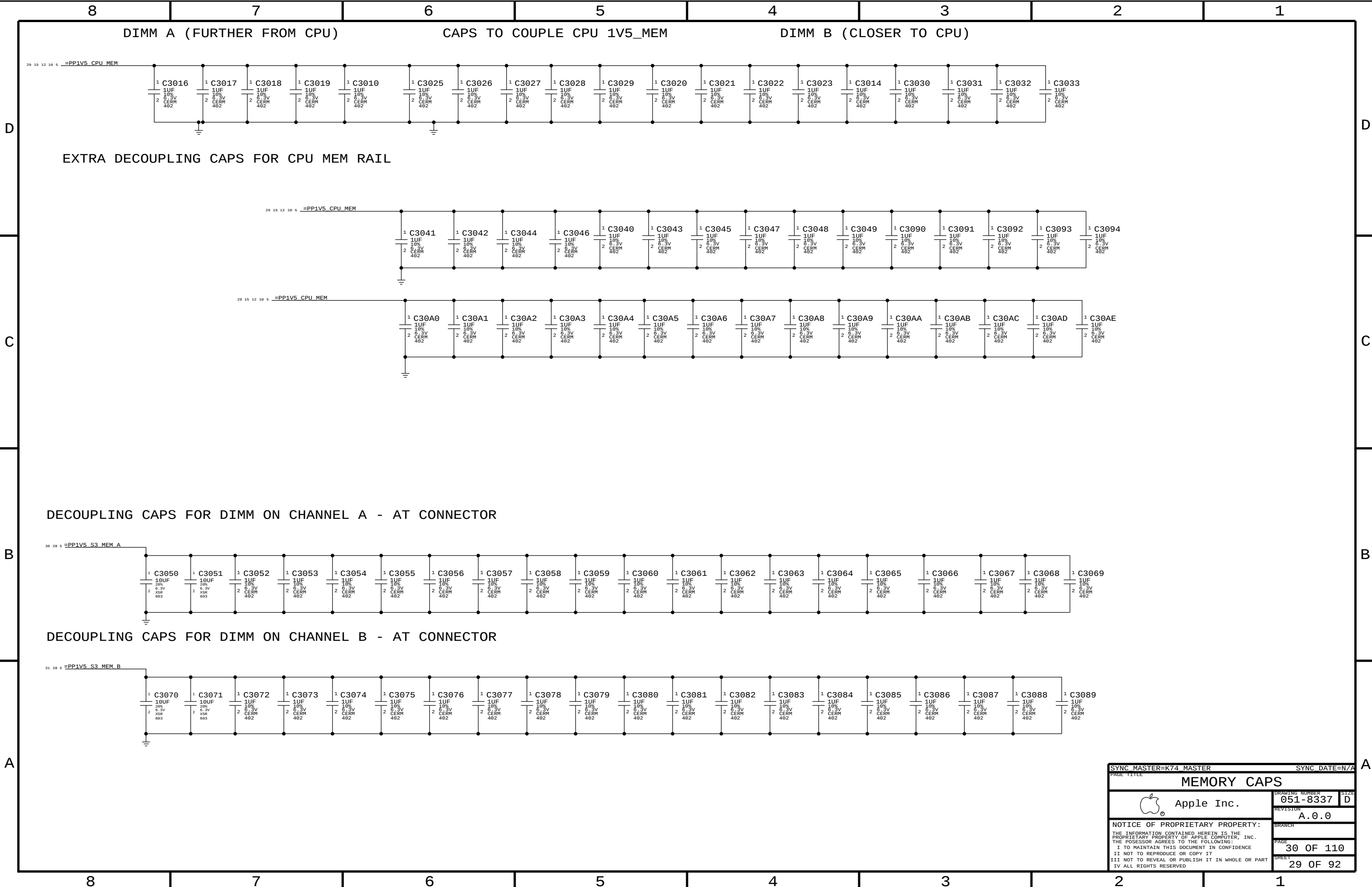


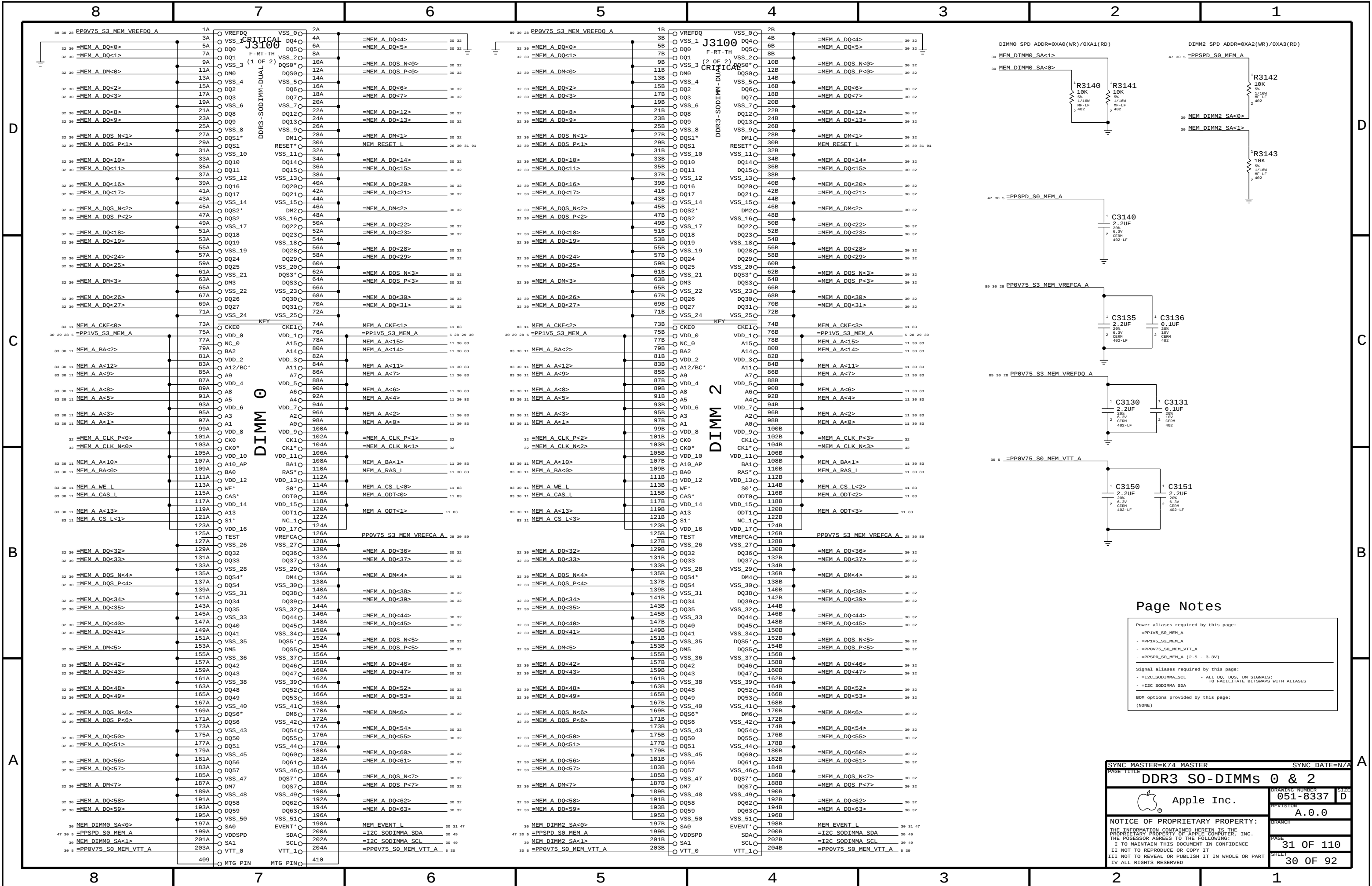
Memory Reset Isolation



	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

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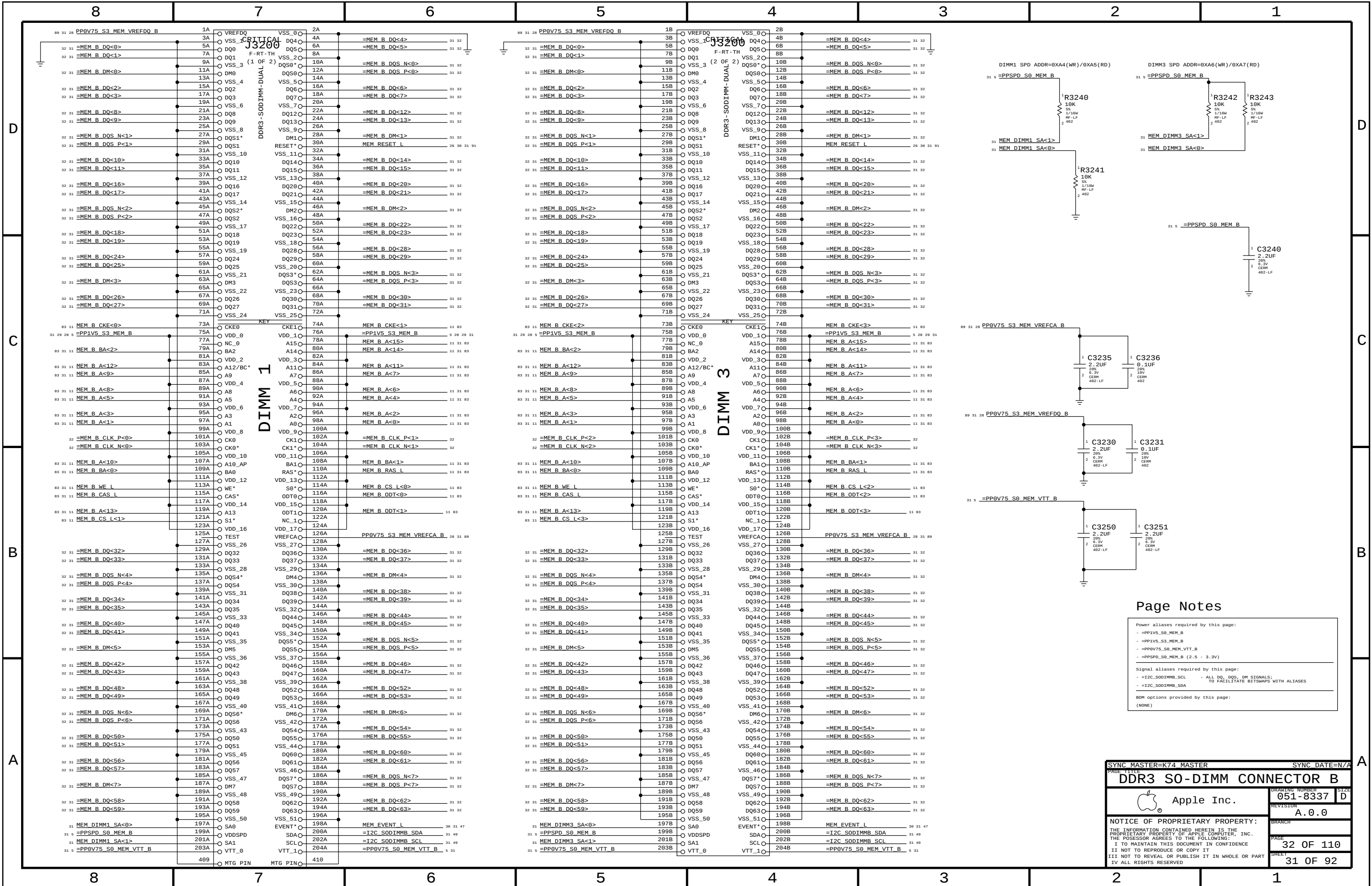




Page Notes

- Power aliases required by this page:
- =PP1V5_S0_MEM_A
 - =PP1V5_S3_MEM_A
 - =PP0V75_S0_MEM_VTT_A
 - =PPSPD_S0_MEM_A (2.5 - 3.3V)
- Signal aliases required by this page:
- =I2C_S0DIMMA_SCL - ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITMAPS WITH ALIASES
 - =I2C_S0DIMMA_SDA
- BOM options provided by this page:
- (NONE)

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE		SIZE	
DDR3 S0-DIMMs 0 & 2		051-8337	
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		A.0.0	
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Page Notes

- Power aliases required by this page:
- =PP1V5_S0_MEM_B
 - =PP1V5_S3_MEM_B
 - =PP0V75_S0_MEM_VTT_B
 - =PPSPD_S0_MEM_B (2.5 - 3.3V)
- Signal aliases required by this page:
- =I2C_SODIMMB_SCL - ALL DQ, DQS, DM SIGNALS;
 - =I2C_SODIMMB_SDA TO FACILITATE BITMAPS WITH ALIASES
- BOM options provided by this page:
- (NONE)

SYNC MASTER=K74 MASTER

SYNC DATE=N/A

DDR3 S0-DIMM CONNECTOR B

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SIZE

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32 OF 110

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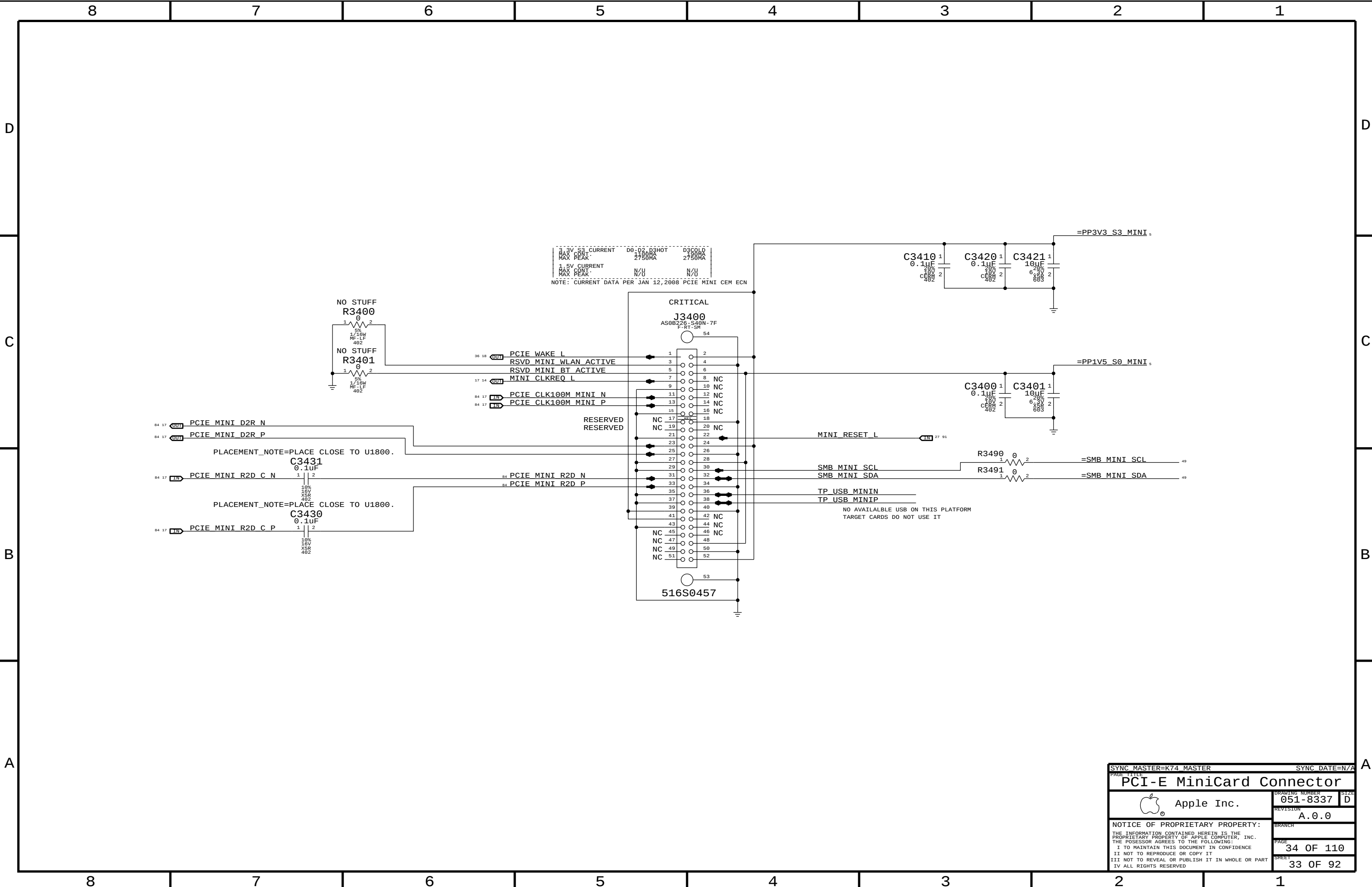
31 OF 92

8		7		6		5		4		3		2		1	
D	CPU CHANNEL A DQS 0 -> DIMM A DQS 7														
	MEM A DQS N<0>	MAKE_BASE=TRUE													
	MEM A DQS P<0>	MAKE_BASE=TRUE													
	MEM A DM<0>	MAKE_BASE=TRUE													
	MEM A DQ<7>	MAKE_BASE=TRUE													
	MEM A DQ<6>	MAKE_BASE=TRUE													
	MEM A DQ<5>	MAKE_BASE=TRUE													
	MEM A DQ<4>	MAKE_BASE=TRUE													
	MEM A DQ<3>	MAKE_BASE=TRUE													
	MEM A DQ<2>	MAKE_BASE=TRUE													
C	CPU CHANNEL A DQS 1 -> DIMM A DQS 6														
	MEM A DQS N<1>	MAKE_BASE=TRUE													
	MEM A DQS P<1>	MAKE_BASE=TRUE													
	MEM A DM<1>	MAKE_BASE=TRUE													
	MEM A DQ<15>	MAKE_BASE=TRUE													
	MEM A DQ<14>	MAKE_BASE=TRUE													
	MEM A DQ<13>	MAKE_BASE=TRUE													
	MEM A DQ<12>	MAKE_BASE=TRUE													
	MEM A DQ<11>	MAKE_BASE=TRUE													
	MEM A DQ<10>	MAKE_BASE=TRUE													
B	CPU CHANNEL A DQS 2 -> DIMM A DQS 5														
	MEM A DQS N<2>	MAKE_BASE=TRUE													
	MEM A DQS P<2>	MAKE_BASE=TRUE													
	MEM A DM<2>	MAKE_BASE=TRUE													
	MEM A DQ<23>	MAKE_BASE=TRUE													
	MEM A DQ<22>	MAKE_BASE=TRUE													
	MEM A DQ<21>	MAKE_BASE=TRUE													
	MEM A DQ<20>	MAKE_BASE=TRUE													
	MEM A DQ<19>	MAKE_BASE=TRUE													
	MEM A DQ<18>	MAKE_BASE=TRUE													
A	CPU CHANNEL A DQS 3 -> DIMM A DQS 4														
	MEM A DQS N<3>	MAKE_BASE=TRUE													
	MEM A DQS P<3>	MAKE_BASE=TRUE													
	MEM A DM<3>	MAKE_BASE=TRUE													
	MEM A DQ<31>	MAKE_BASE=TRUE													
	MEM A DQ<30>	MAKE_BASE=TRUE													
	MEM A DQ<29>	MAKE_BASE=TRUE													
	MEM A DQ<28>	MAKE_BASE=TRUE													
	MEM A DQ<27>	MAKE_BASE=TRUE													
	MEM A DQ<26>	MAKE_BASE=TRUE													

MEMORY CLOCK ALIASING

MEM A CLK P<0>	MAKE_BASE=TRUE													
MEM A CLK N<0>	MAKE_BASE=TRUE													
MEM A CLK P<1>	MAKE_BASE=TRUE													
MEM A CLK N<1>	MAKE_BASE=TRUE													
MEM A CLK P<2>	MAKE_BASE=TRUE													
MEM A CLK N<2>	MAKE_BASE=TRUE													
MEM A CLK P<3>	MAKE_BASE=TRUE													
MEM A CLK N<3>	MAKE_BASE=TRUE													
MEM B CLK P<0>	MAKE_BASE=TRUE													
MEM B CLK N<0>	MAKE_BASE=TRUE													
MEM B CLK P<1>	MAKE_BASE=TRUE													
MEM B CLK N<1>	MAKE_BASE=TRUE													
MEM B CLK P<2>	MAKE_BASE=TRUE													
MEM B CLK N<2>	MAKE_BASE=TRUE													
MEM B CLK P<3>	MAKE_BASE=TRUE													
MEM B CLK N<3>	MAKE_BASE=TRUE													

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE		SIZE	
DDR3 ALIAS AND BITSWAPS		051-8337	
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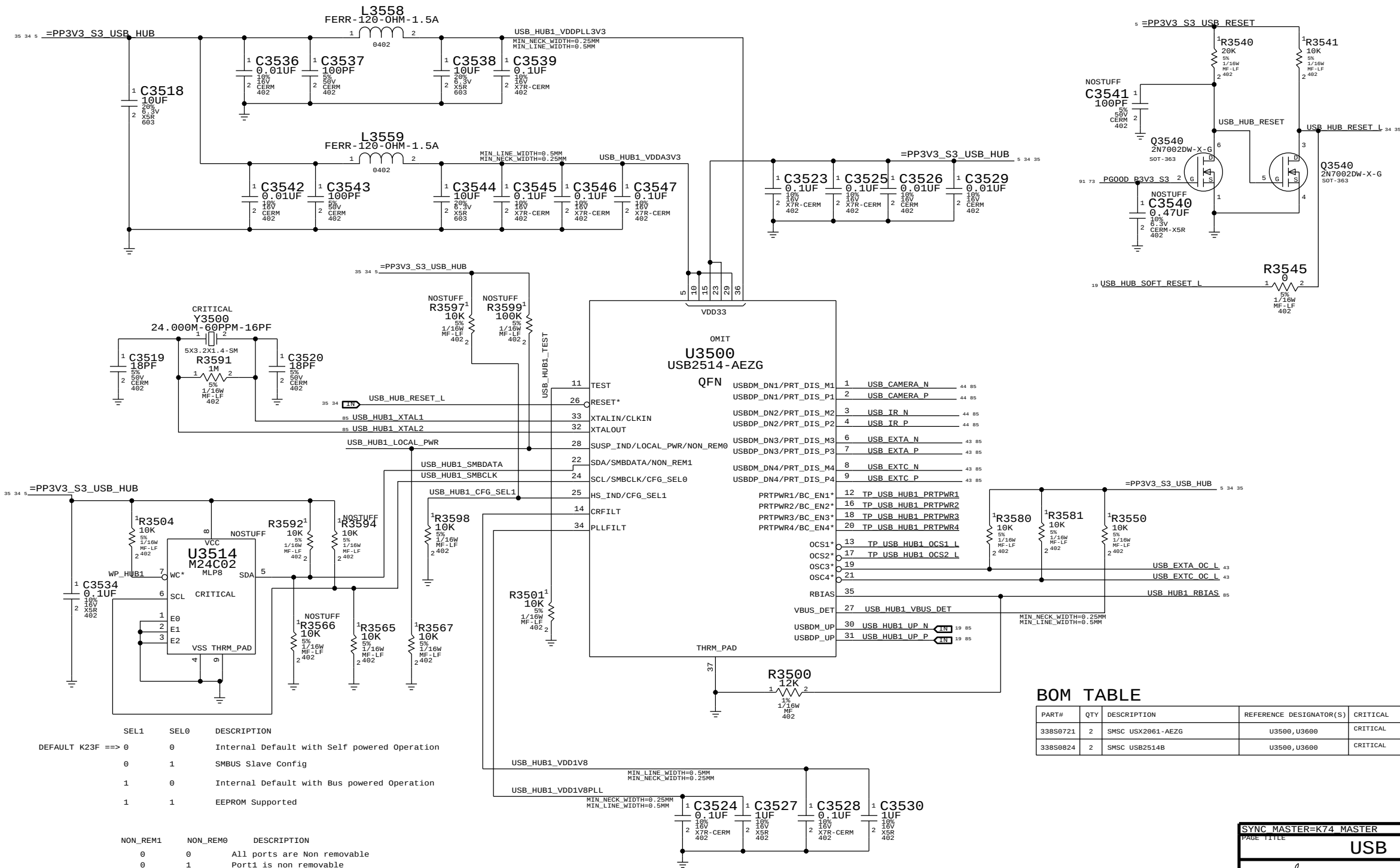
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B

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USB HUB - 1



SYNC MASTER=K74 MASTER

SYNC DATE=N/A

USB HUB 1

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051-8337

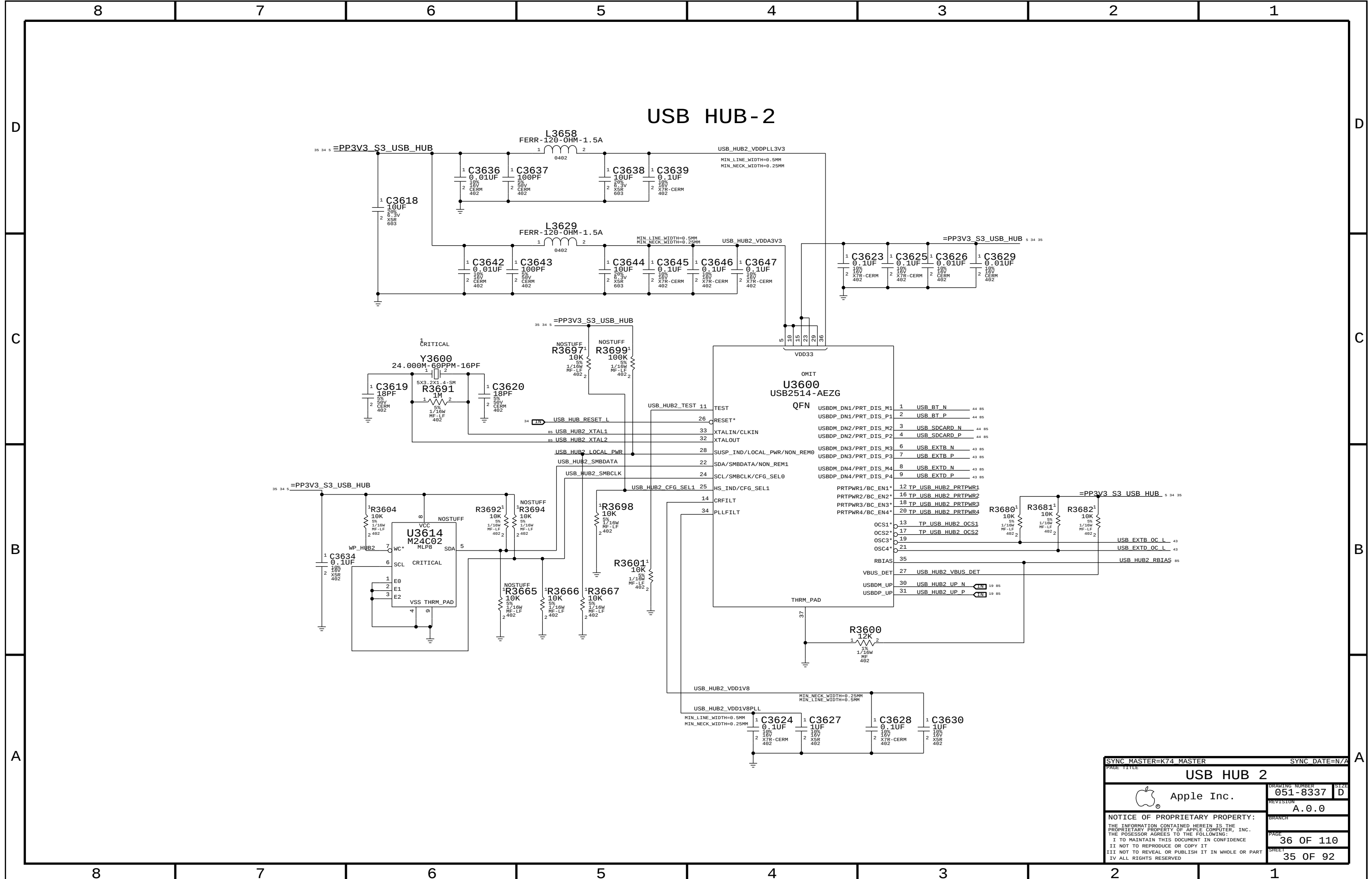
A.0.0

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34 OF 92

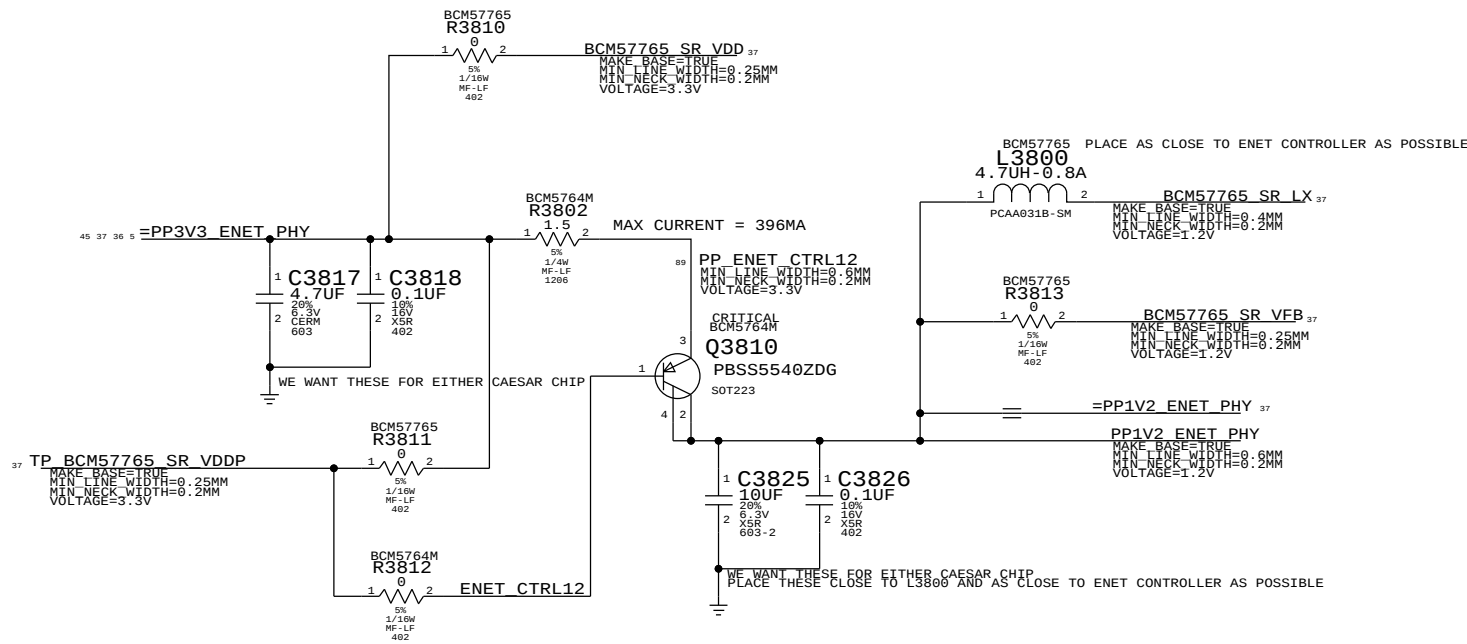
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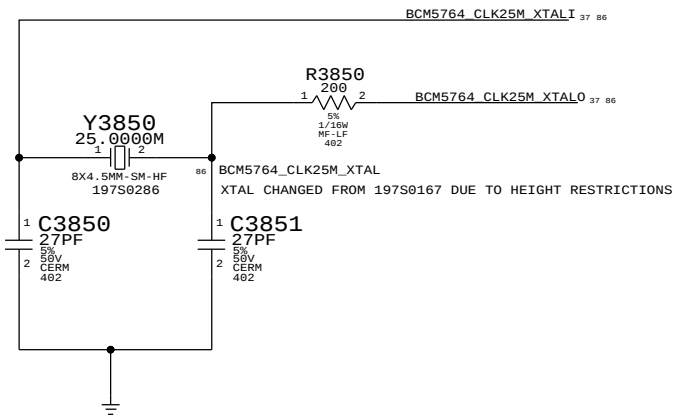


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PAGE TITLE			
USB HUB 2			
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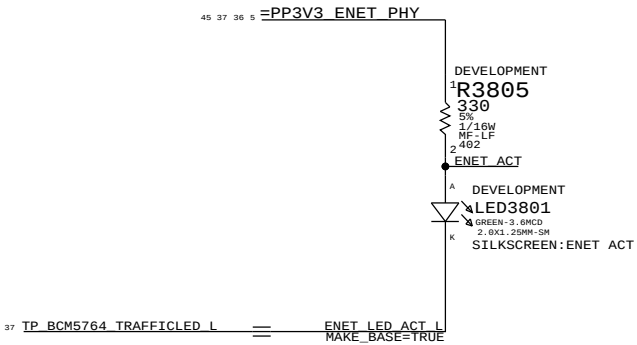
CAESAR II/IV 1V2 RAIL SUPPLY



CAESAR II/IV 25MHZ XTAL

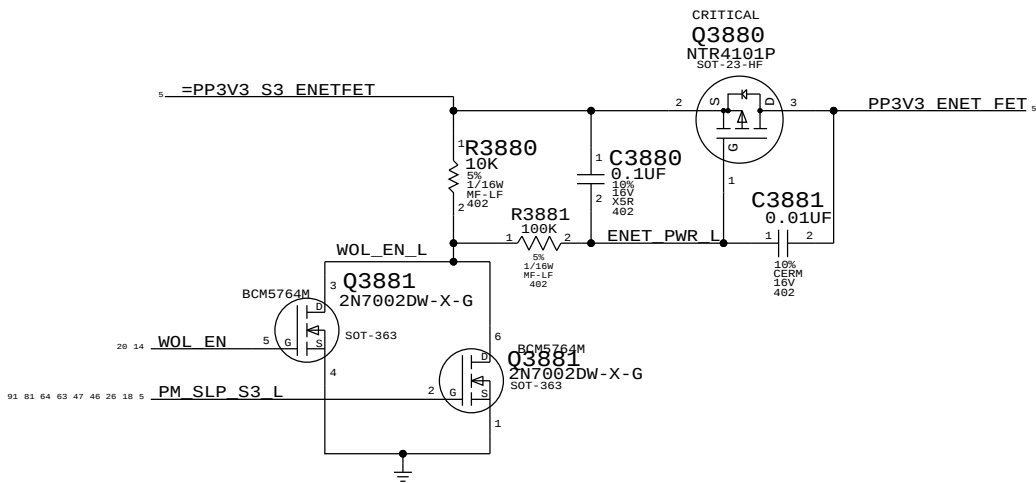


CAESAR II/IV ACTIVITY LED

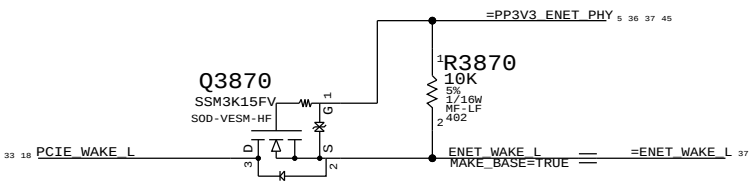


3.3V ENET FET

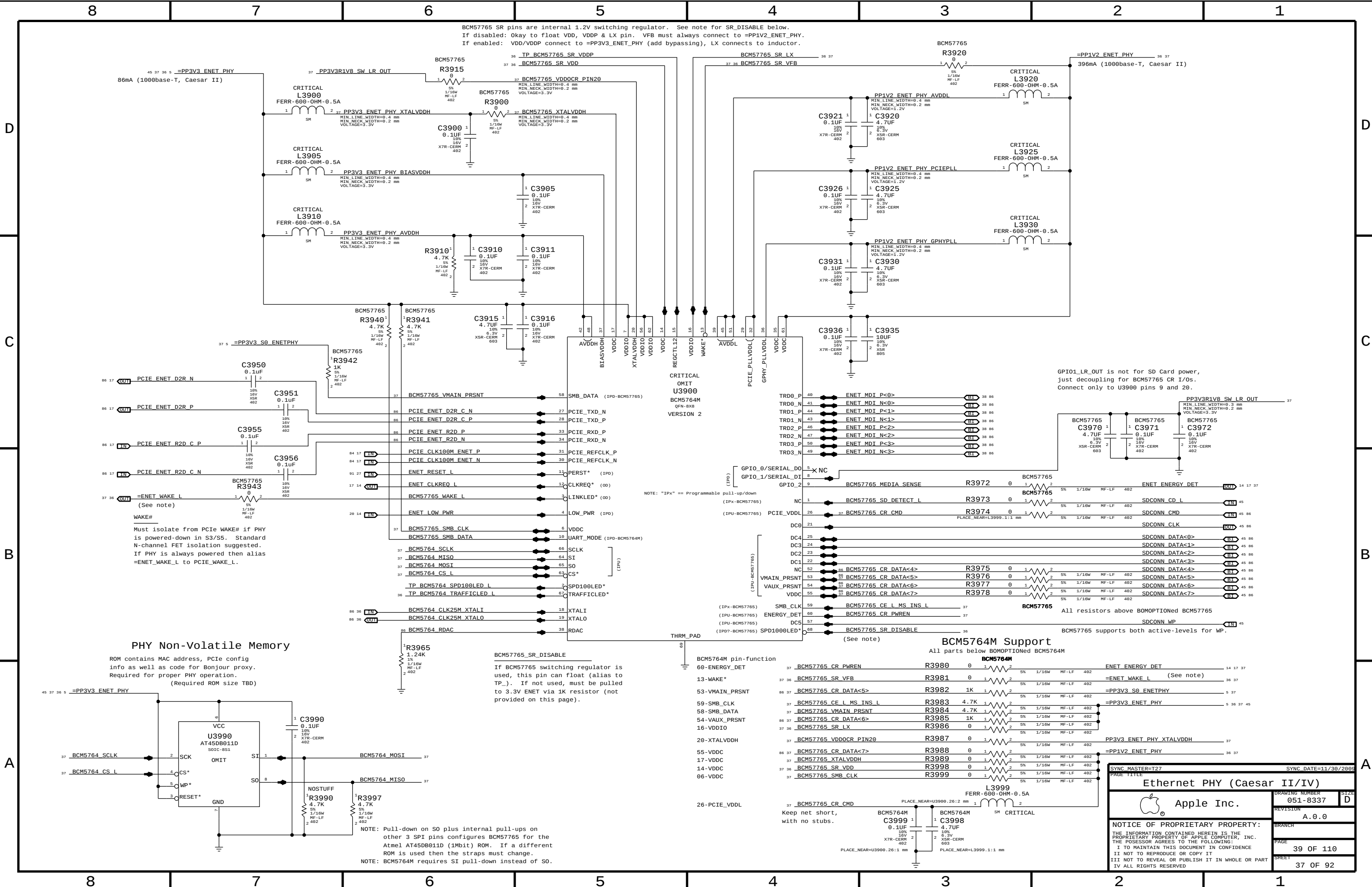
ENET_PWR_ON = "S0" || (S3 power && WOL_EN)



CAESAR II/IV WAKE# ISOLATION



SYNC MASTER=MASTER		SYNC DATE=N/A	
PAGE TITLE		Caesar II/IV Support	
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PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.

(Required ROM size TBD)

BCM57765_SR_DISABLE

If BCM57765 switching regulator is used, this pin can float (alias to TP...). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

BCM5764M Support

All parts below BOMOPTIONed BCM5764M

BCM5764M		BCM57765	
60-ENERGY_DET	BCM57765 CR PWREN	R3980	0 1/16W MF-LF 402
13-WAKE*	BCM57765 SR VFB	R3981	0 1/16W MF-LF 402
53-VMAIN_PRSN	BCM57765 CR DATA<5>	R3982	1K 1/16W MF-LF 402
59-SMB_CLK	BCM57765 CE L MS INS L	R3983	4.7K 1/16W MF-LF 402
58-SMB_DATA	BCM57765 VMAIN_PRSN	R3984	4.7K 1/16W MF-LF 402
54-VAUX_PRSN	BCM57765 CR DATA<6>	R3985	1K 1/16W MF-LF 402
16-VDDIO	BCM57765 SR LX	R3986	0 1/16W MF-LF 402
20-XTALVDDH	BCM57765 VDDOCR PIN20	R3987	0 1/16W MF-LF 402
55-VDDC	BCM57765 CR DATA<7>	R3988	0 1/16W MF-LF 402
17-VDDC	BCM57765 XTALVDDH	R3989	0 1/16W MF-LF 402
14-VDDC	BCM57765 SR VDD	R3990	0 1/16W MF-LF 402
06-VDDC	BCM57765 SMB_CLK	R3999	0 1/16W MF-LF 402

BCM5764M		BCM57765	
Keep net short, with no stubs.	BCM5764M C3999	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3998	4.7uF	10% 6.3V XSR-CERM 603
	BCM5764M C3997	4.7uF	10% 6.3V XSR-CERM 603
	BCM5764M C3996	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3995	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3994	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3993	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3992	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3991	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3990	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3989	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3988	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3987	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3986	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3985	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3984	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3983	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3982	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3981	0.1uF	10% 16V X7R-CERM 402
	BCM5764M C3980	0.1uF	10% 16V X7R-CERM 402

SYNC MASTER=T27

SYNC DATE=11/30/2008

Ethernet PHY (Caesar II/IV)

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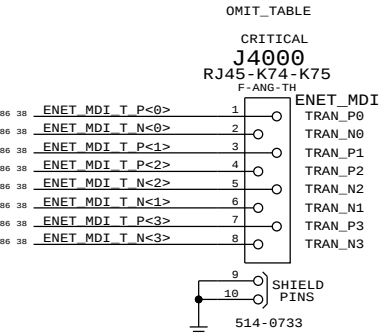
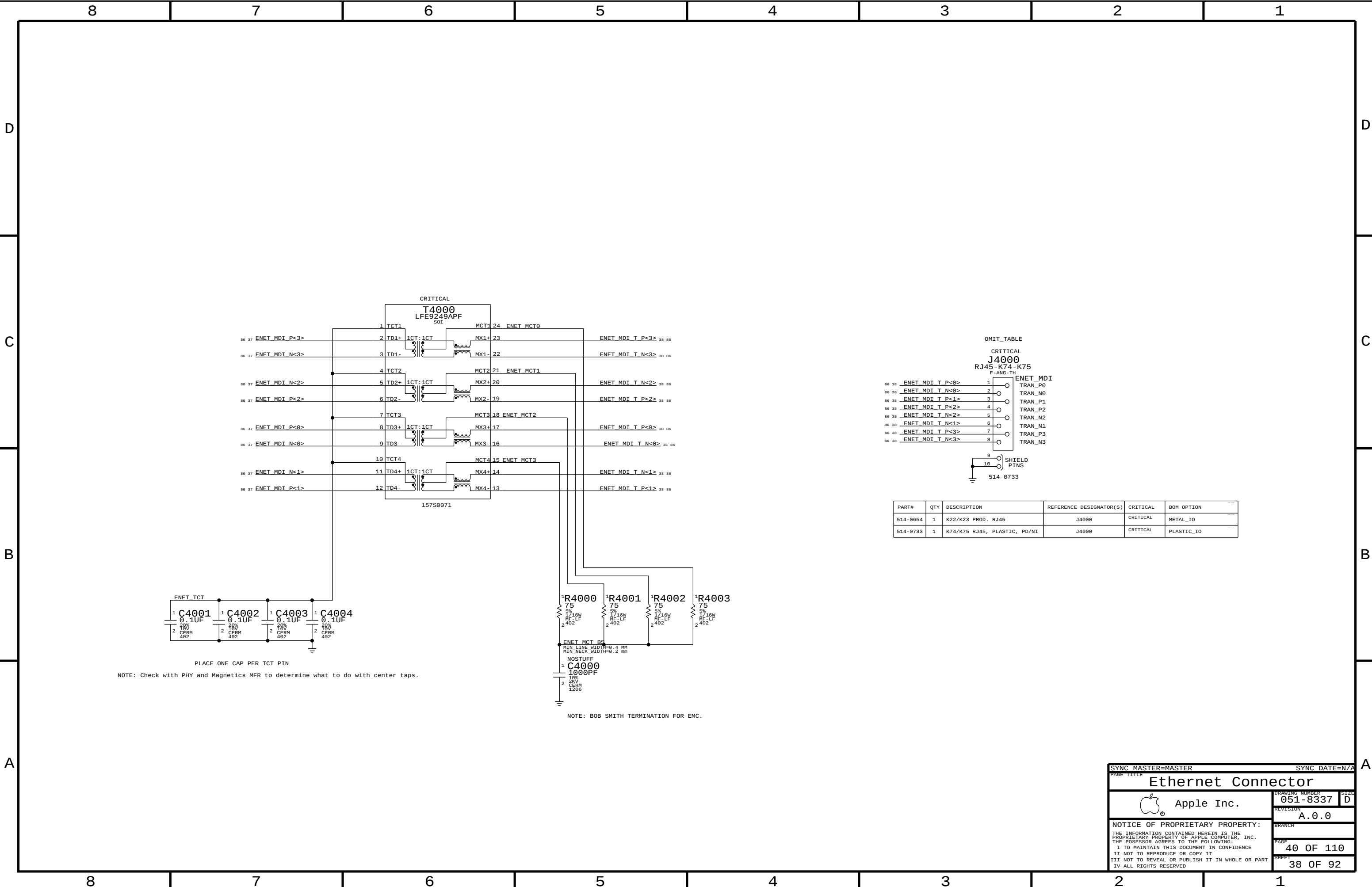
39 OF 110

SHEET

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GPI01_LR_OUT is not for SD Card power, just decoupling for BCM57765 CR I/Os. Connect only to U3900 pins 9 and 20.

All resistors above BOMOPTIONed BCM57765
BCM57765 supports both active-levels for WP.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0654	1	K22/K23 PROD. RJ45	J4000	CRITICAL	METAL_IO
514-0733	1	K74/K75 RJ45, PLASTIC, PD/NI	J4000	CRITICAL	PLASTIC_IO

PLACE ONE CAP PER TCT PIN

NOTE: Check with PHY and Magnetics MFR to determine what to do with center taps.

SYNC MASTER=MASTER

SYNC DATE=N/A

Ethernet Connector

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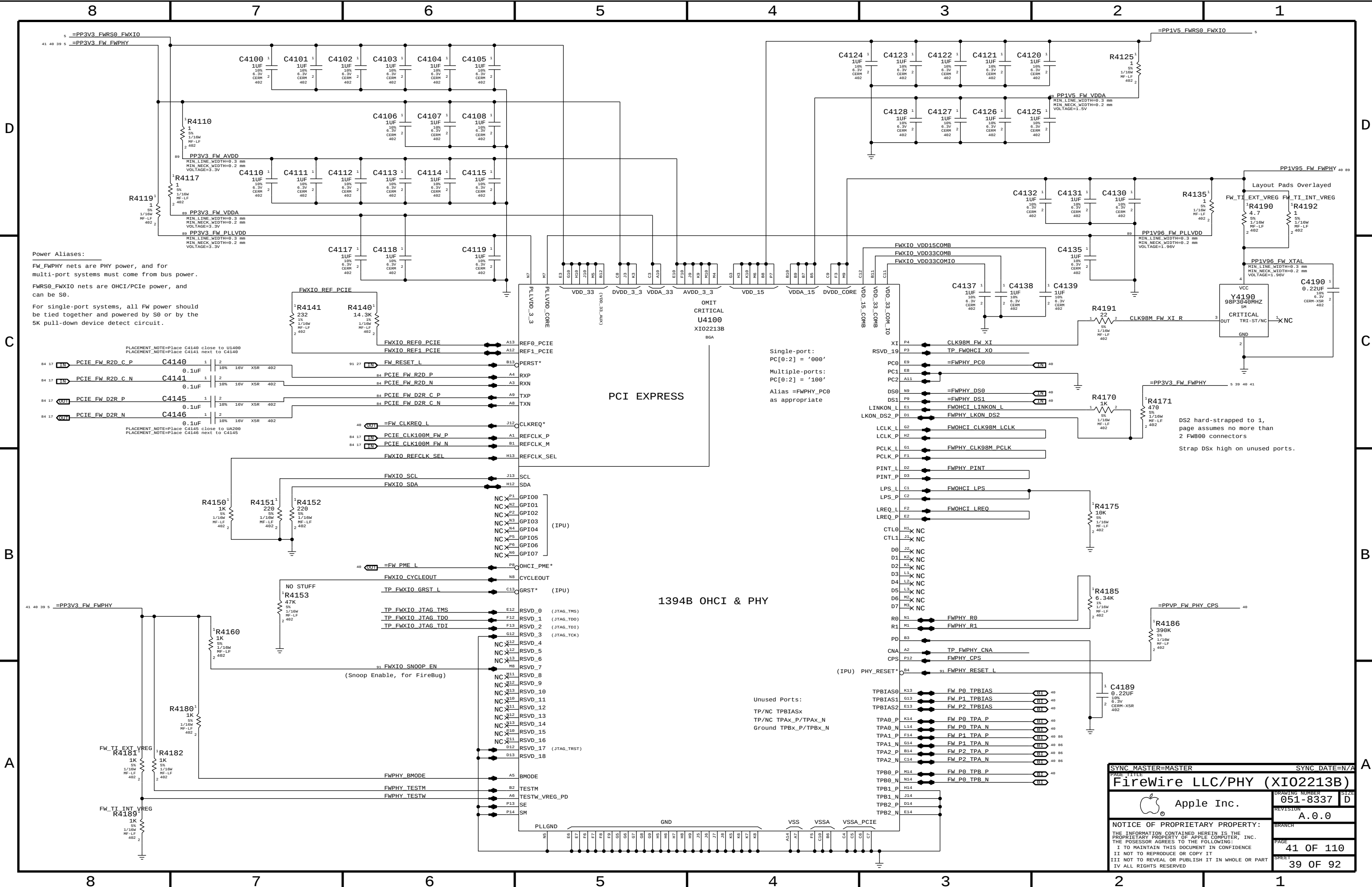
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PAGE

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5 =PP3V3 FWRS0 FWXIO
41 40 39 5 =PP3V3 FW FWPHY

=PP1V5 FWRS0 FWXIO 5

Power Aliases:
FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.
FWRS0_FWXIO nets are OHCI/PCIE power, and can be S0.
For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.

PLACEMENT_NOTE=Place C4140 close to U1400
PLACEMENT_NOTE=Place C4141 next to C4140

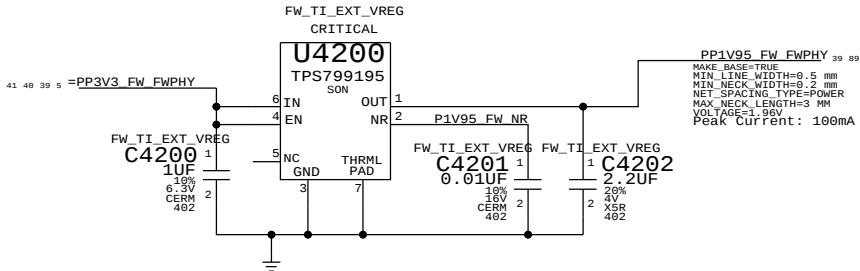
PLACEMENT_NOTE=Place C4145 close to UA200
PLACEMENT_NOTE=Place C4146 next to C4145

Single-port:
PC[0:2] = '000'
Multiple-ports:
PC[0:2] = '100'
Alias =FWPHY_PC0
as appropriate

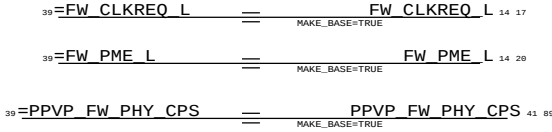
DS2 hard-strapped to 1,
page assumes no more than
2 FW000 connectors
Strap DSx high on unused ports.

SYNC MASTER=MASTER		SYNC DATE=N/A	
PAGE TITLE		FireWire LLC/PHY (XIO2213B)	
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		REVISION	A.0.0
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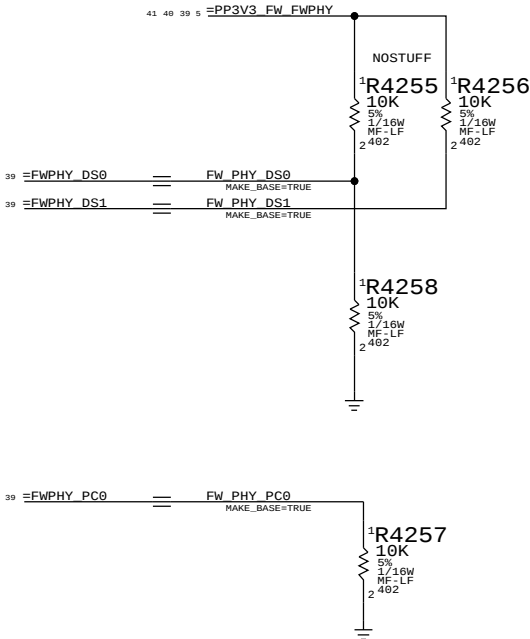
1394 PHY 1.95V SUPPLY



FireWire Aliases For Connectivity



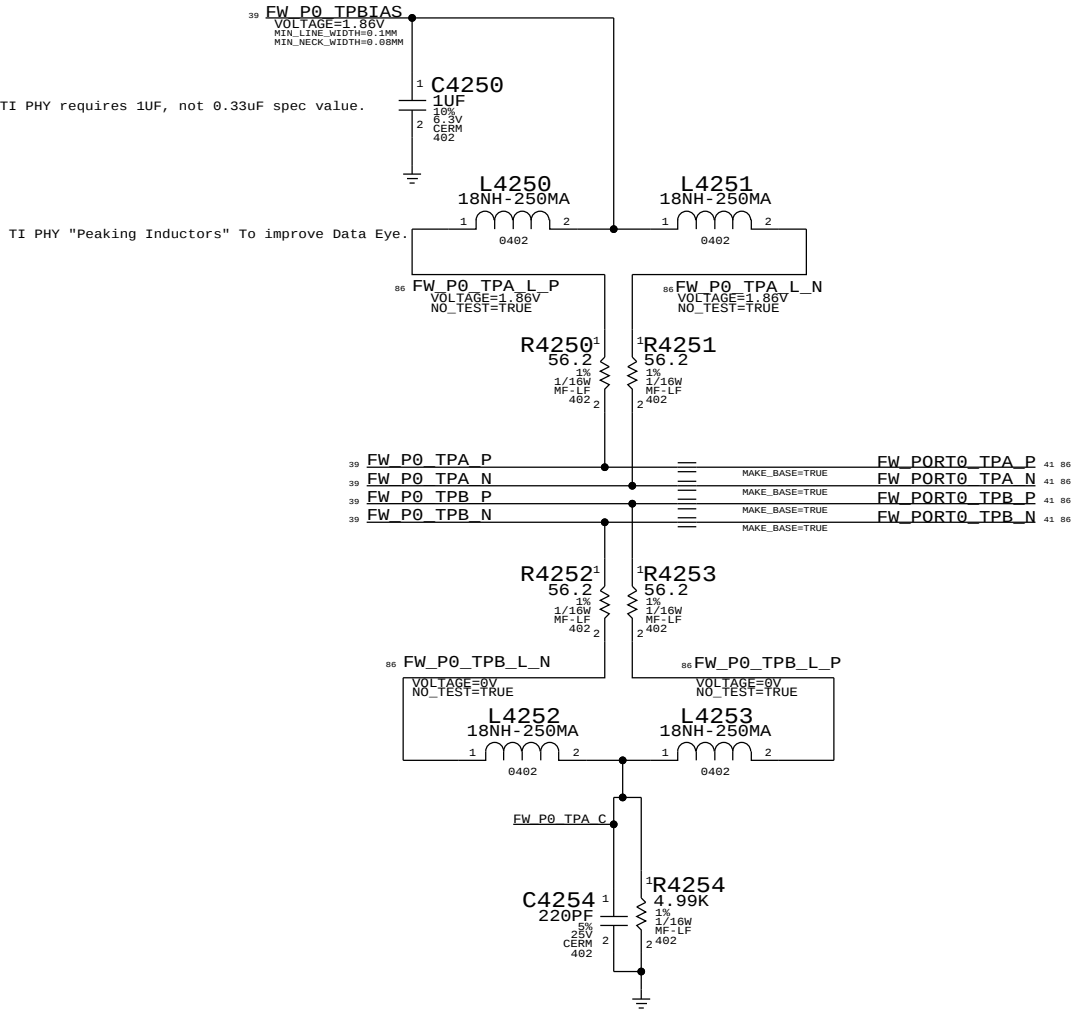
1394 PHY STRAPPING OPTIONS



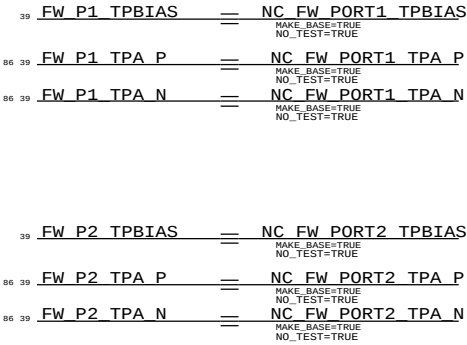
THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

iMacs are now one port only and have Power Code "000"

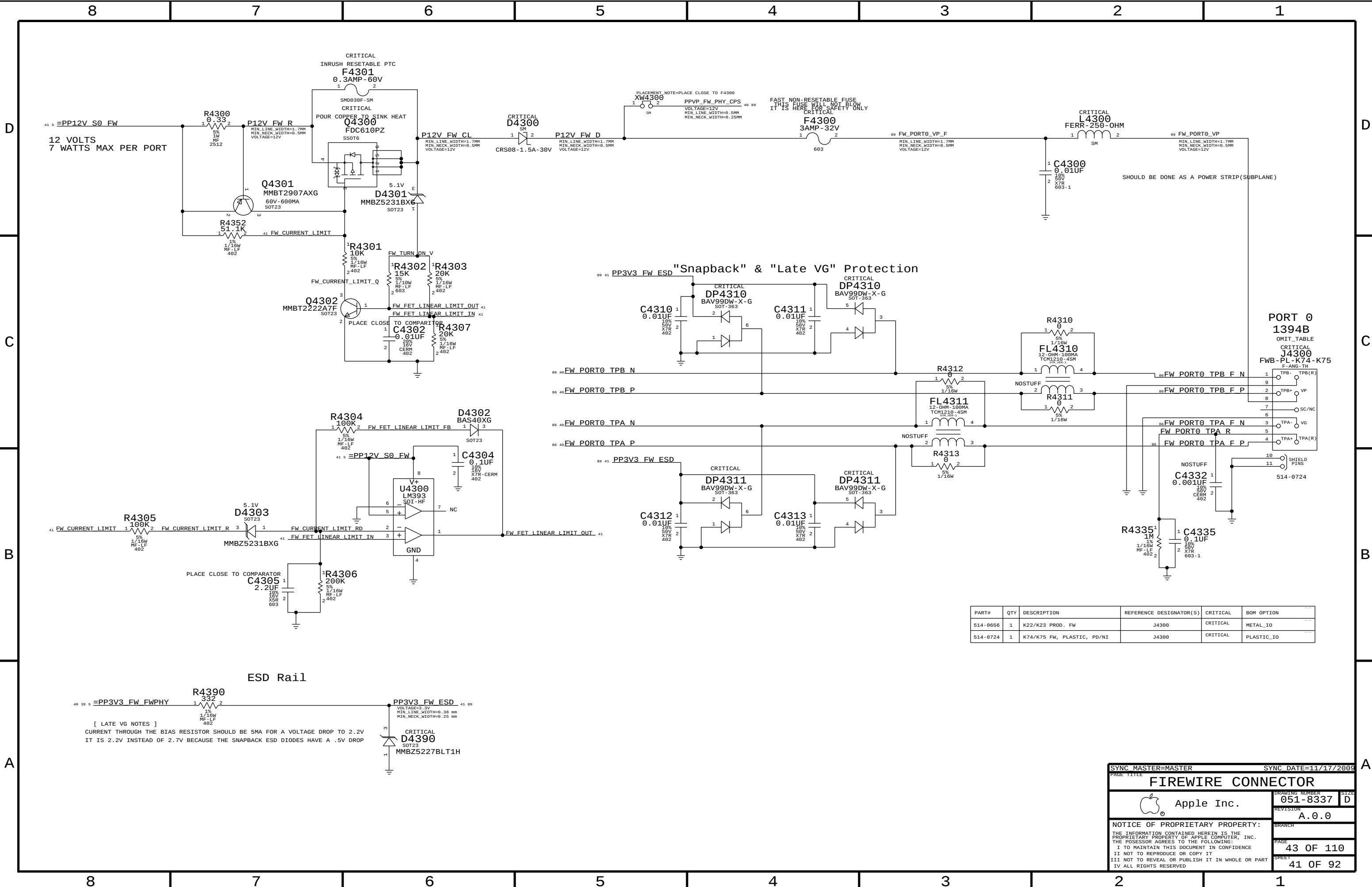
Termination
Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED

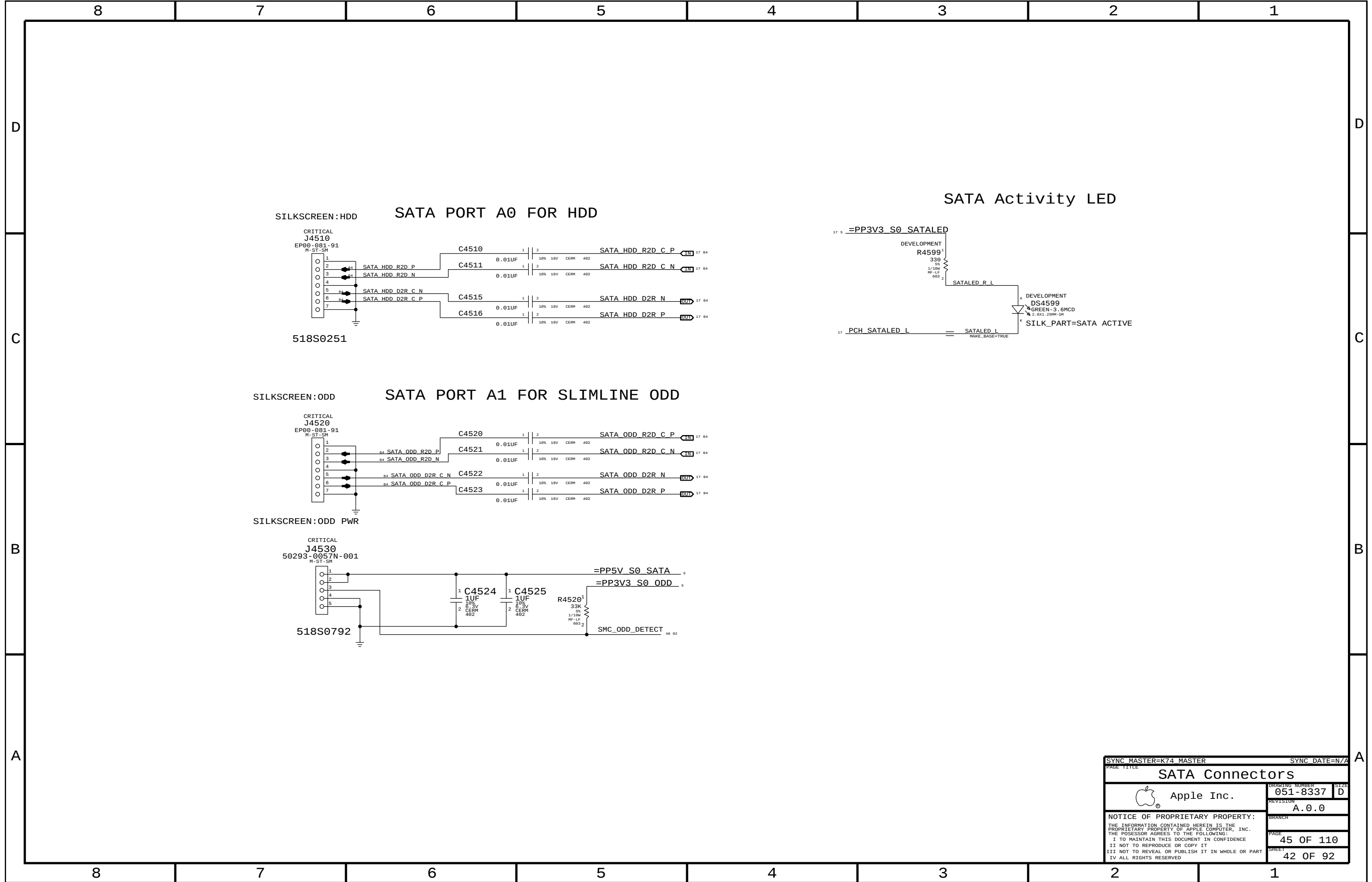


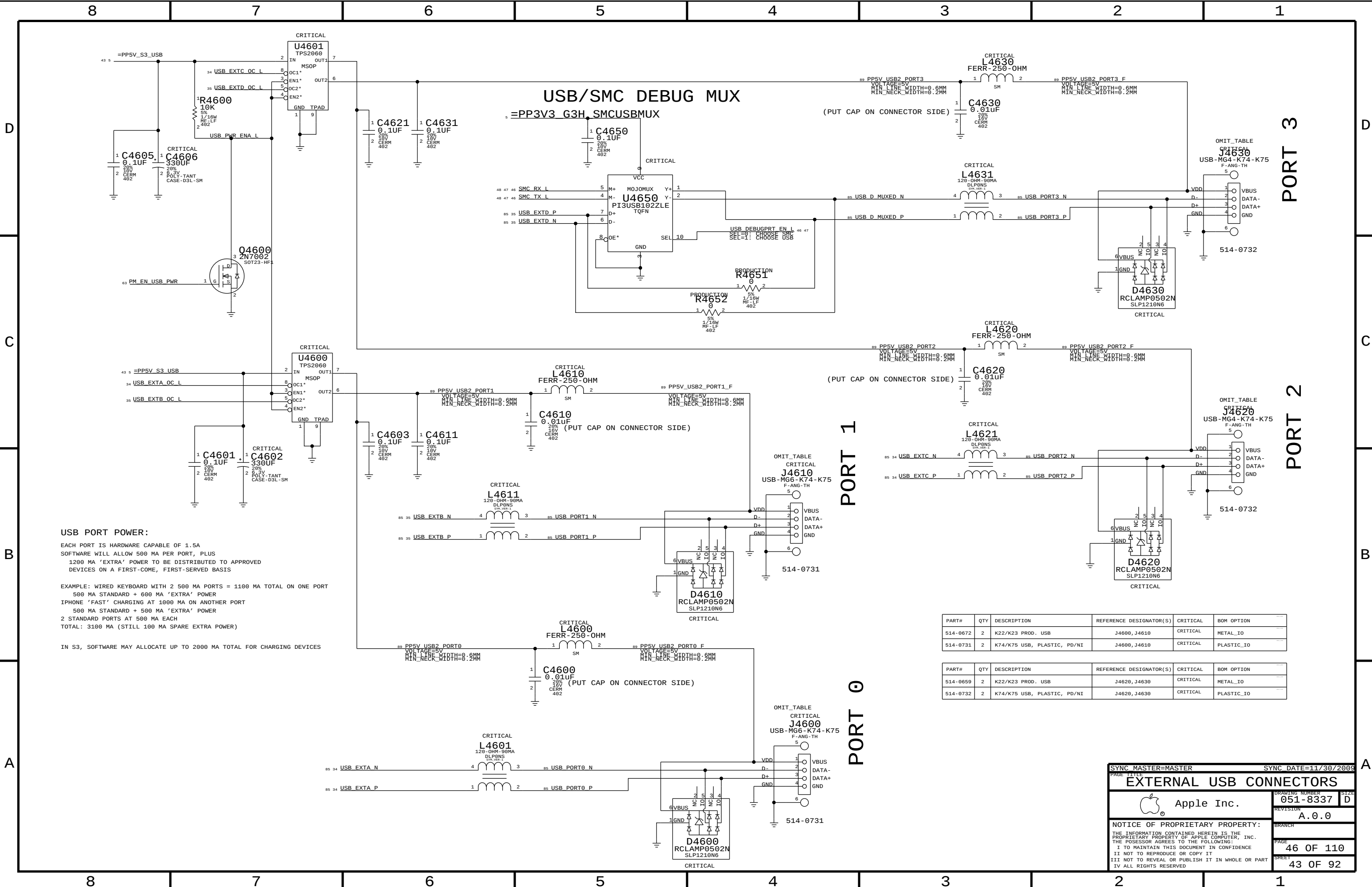
SYNC MASTER=MASTER		SYNC DATE=N/A	
PAGE TITLE		FW: 1394B MISC	
DRAWING NUMBER		051-8337	SIZE D
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USB PORT POWER:

EACH PORT IS HARDWARE CAPABLE OF 1.5A
SOFTWARE WILL ALLOW 500 MA PER PORT, PLUS
1200 MA 'EXTRA' POWER TO BE DISTRIBUTED TO APPROVED
DEVICES ON A FIRST-COME, FIRST-SERVED BASIS

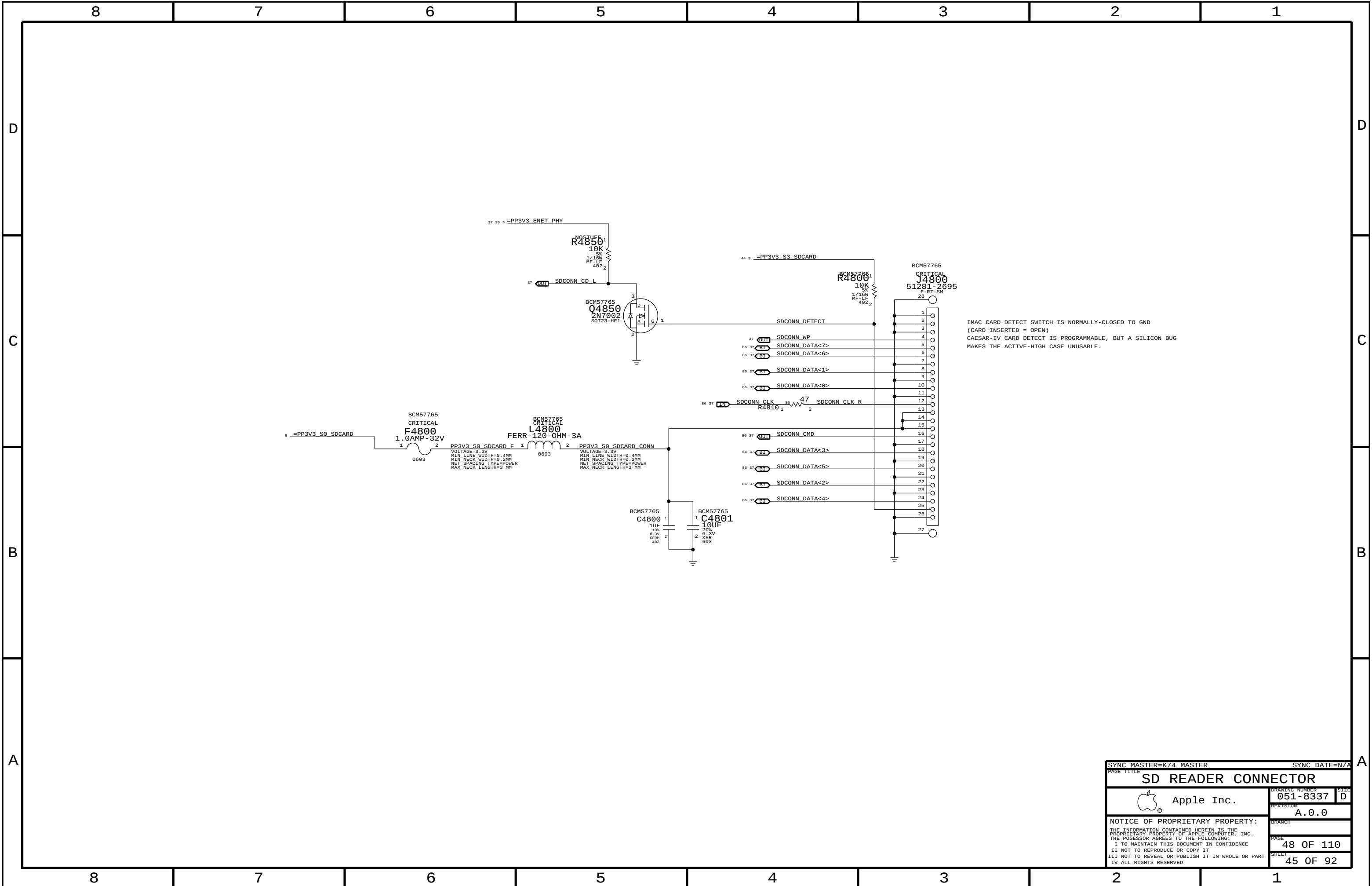
EXAMPLE: WIRED KEYBOARD WITH 2 500 MA PORTS = 1100 MA TOTAL ON ONE PORT
500 MA STANDARD + 600 MA 'EXTRA' POWER
IPHONE 'FAST' CHARGING AT 1000 MA ON ANOTHER PORT
500 MA STANDARD + 500 MA 'EXTRA' POWER
2 STANDARD PORTS AT 500 MA EACH
TOTAL: 3100 MA (STILL 100 MA SPARE EXTRA POWER)

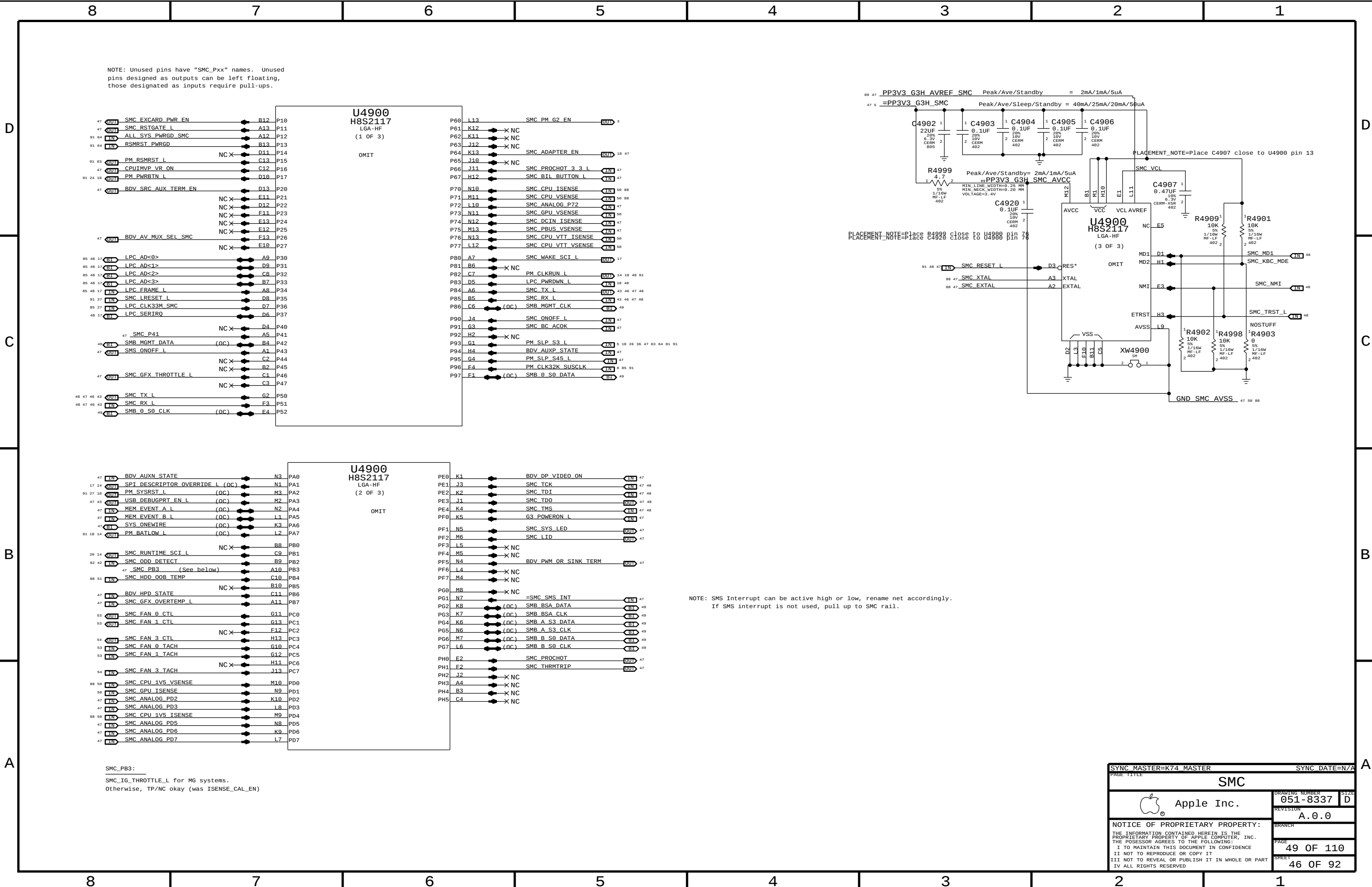
IN S3, SOFTWARE MAY ALLOCATE UP TO 2000 MA TOTAL FOR CHARGING DEVICES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0672	2	K22/K23 PROD. USB	J4600, J4610	CRITICAL	METAL_IO
514-0731	2	K74/K75 USB, PLASTIC, PD/NI	J4600, J4610	CRITICAL	PLASTIC_IO

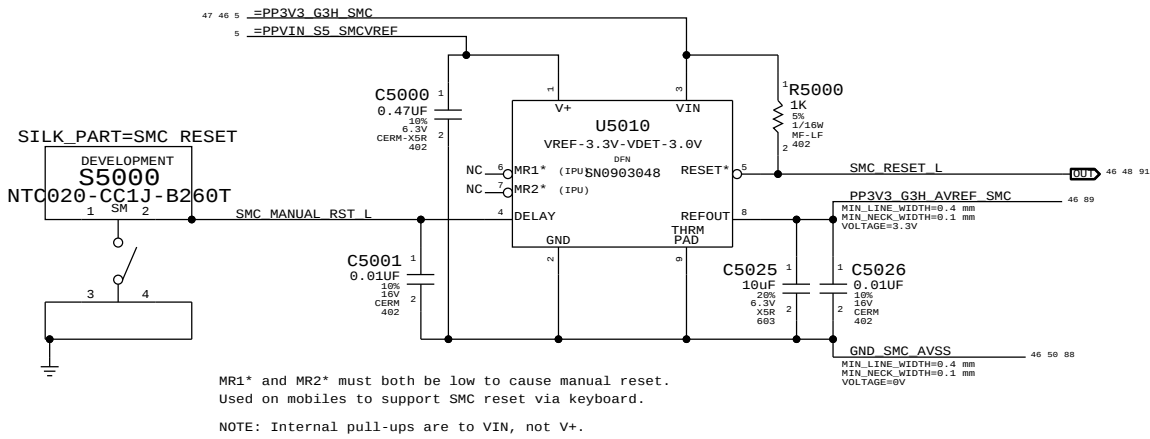
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0659	2	K22/K23 PROD. USB	J4620, J4630	CRITICAL	METAL_IO
514-0732	2	K74/K75 USB, PLASTIC, PD/NI	J4620, J4630	CRITICAL	PLASTIC_IO

SYNC MASTER=MASTER		SYNC DATE=11/30/2009	
PAGE TITLE		EXTERNAL USB CONNECTORS	
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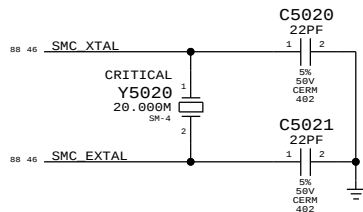


SMC Reset "Button", Supervisor & AVREF Supply

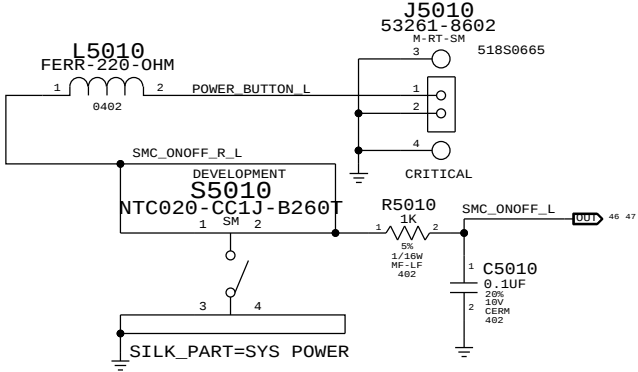


MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

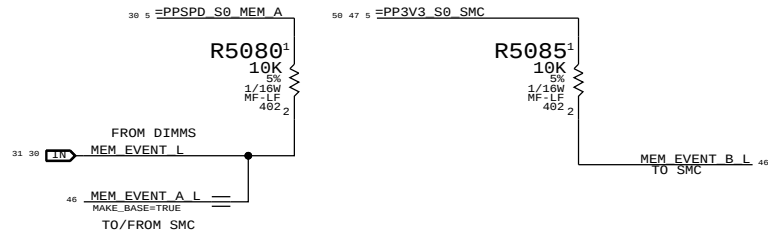
SMC Crystal Circuit



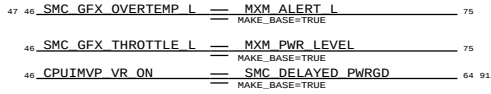
POWER BUTTON



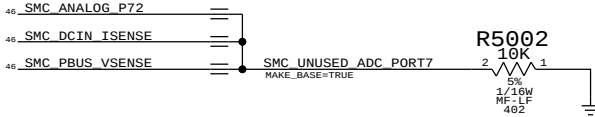
MEM_EVENT



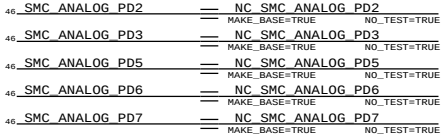
MISC. SIGNAL ALIASES



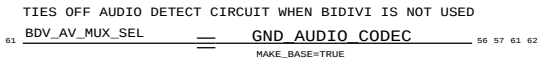
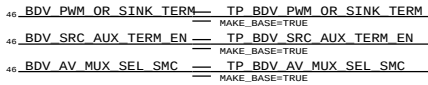
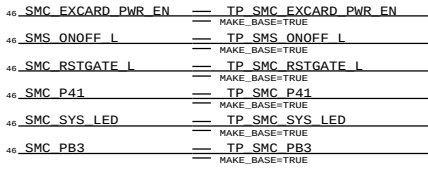
UNUSED PORT 7 ANALOG SENSORS



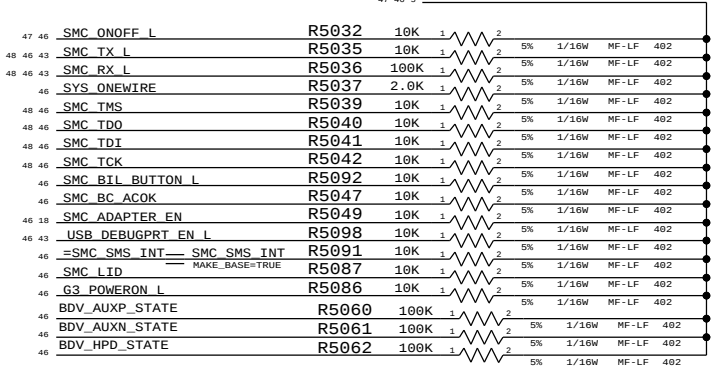
UNUSED PORT D ANALOG (INTERNAL PULLUPS)



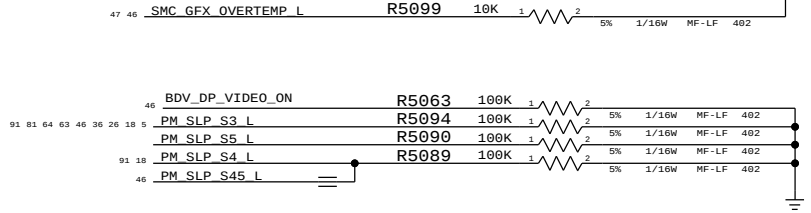
UNUSED TP/NC ALIASES



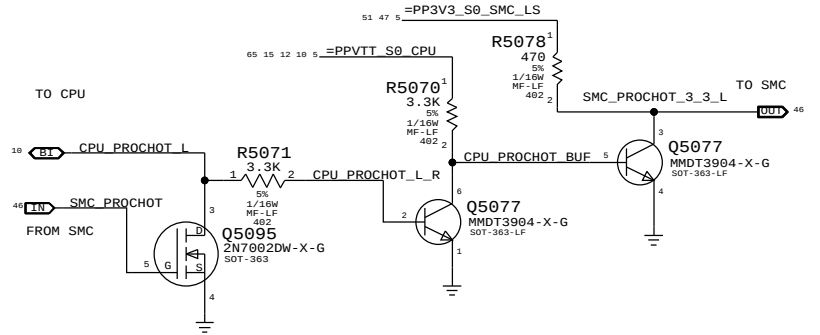
=PP3V3_G3H_SMC



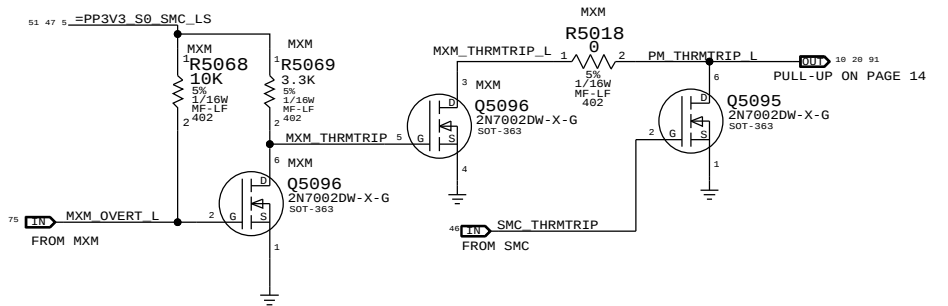
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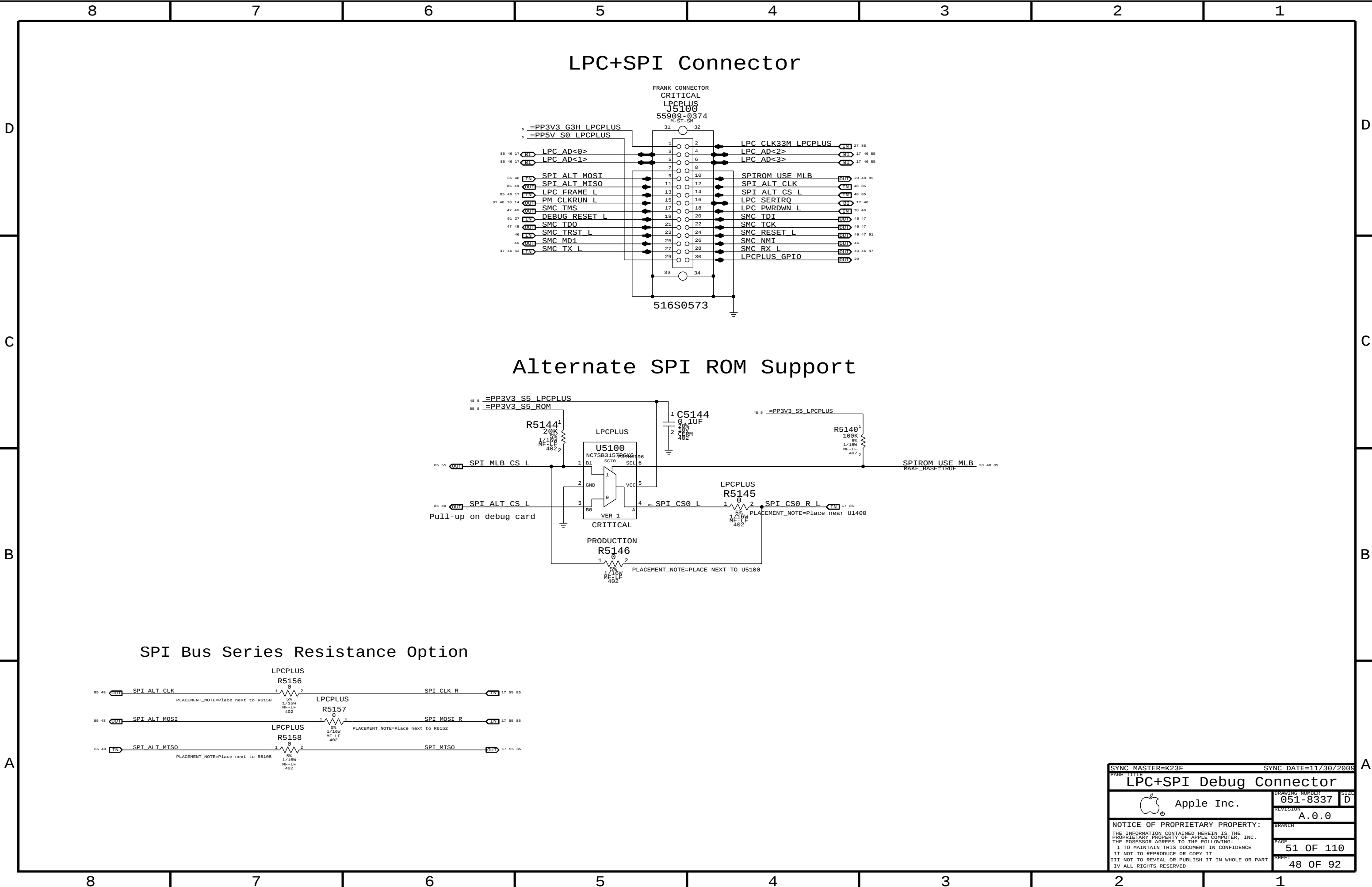
SMC PROCHOT 3.3V LEVEL SHIFTING

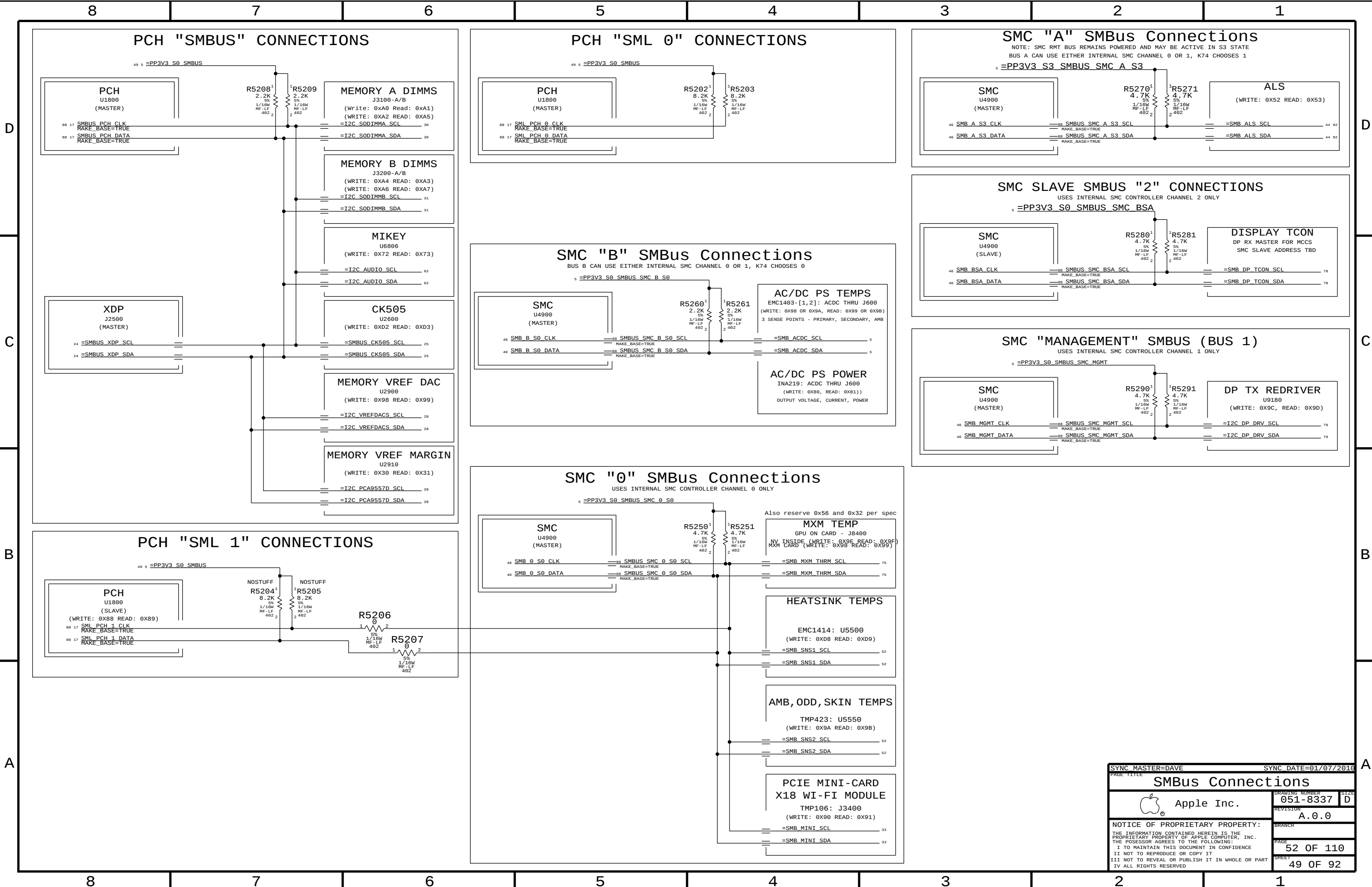


SMC & MXM THERMTRIP LEVEL SHIFTING

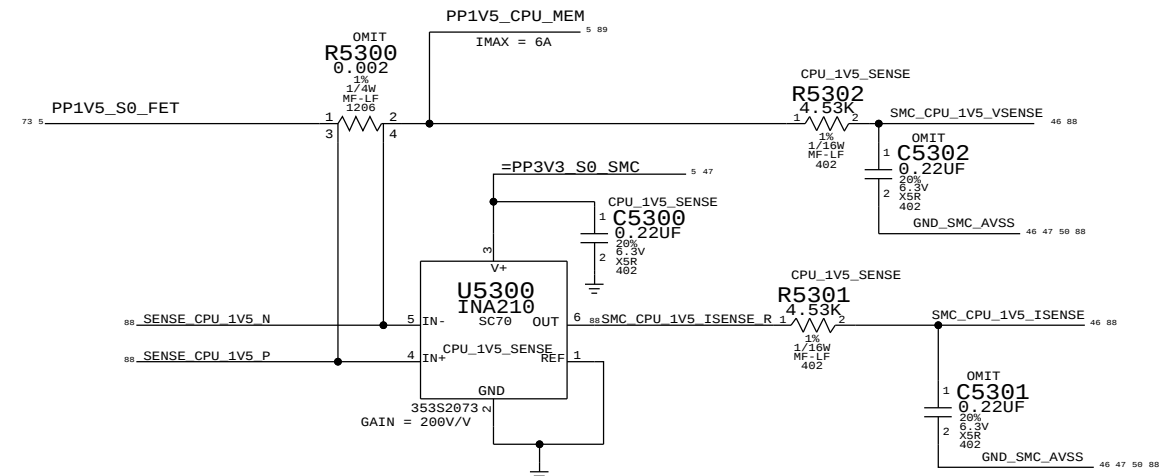


SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
SMC Support			
Apple Inc.		DRAWING NUMBER	051-8337
		REVISION	A.0.0
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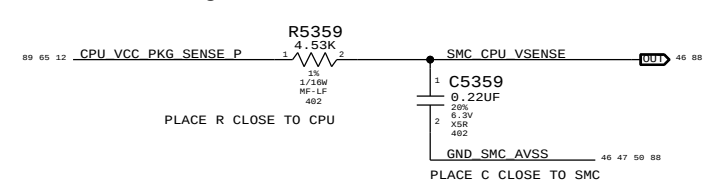
CPU 1.5V CURRENT SENSE



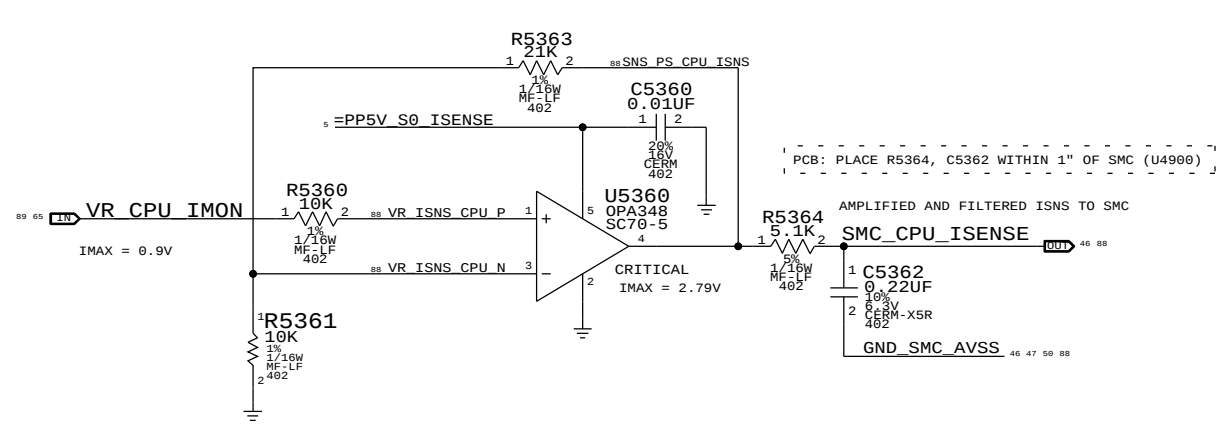
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES, 2 MILLIOHM, 1206	R5300	CPU_1V5_SENSE
101S0414	1	RES, 0 OHM, 1206, 20 MILLIOHM MAX	R5300	PRODUCTION
132S0080	2	CAP, 0.22UF, 402	C5301, C5302	CPU_1V5_SENSE
116S0004	2	RES, 0 OHM, 402	C5301, C5302	PRODUCTION

CPU 1.5V VOLTAGE SENSE

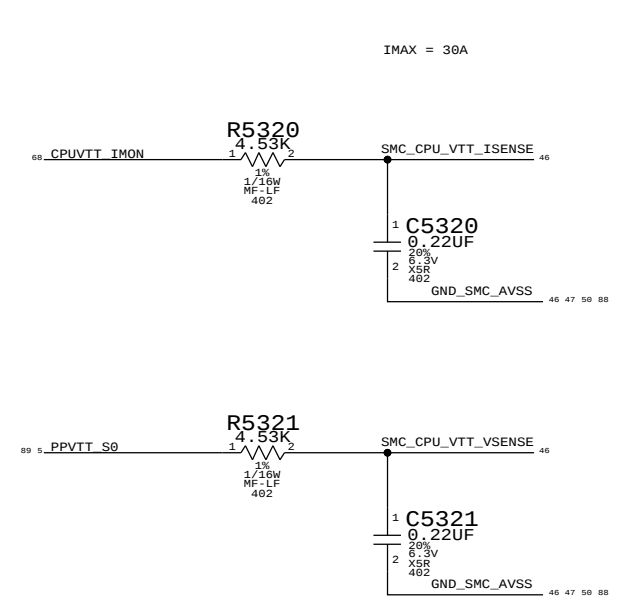
CPU Voltage Sense / Filter



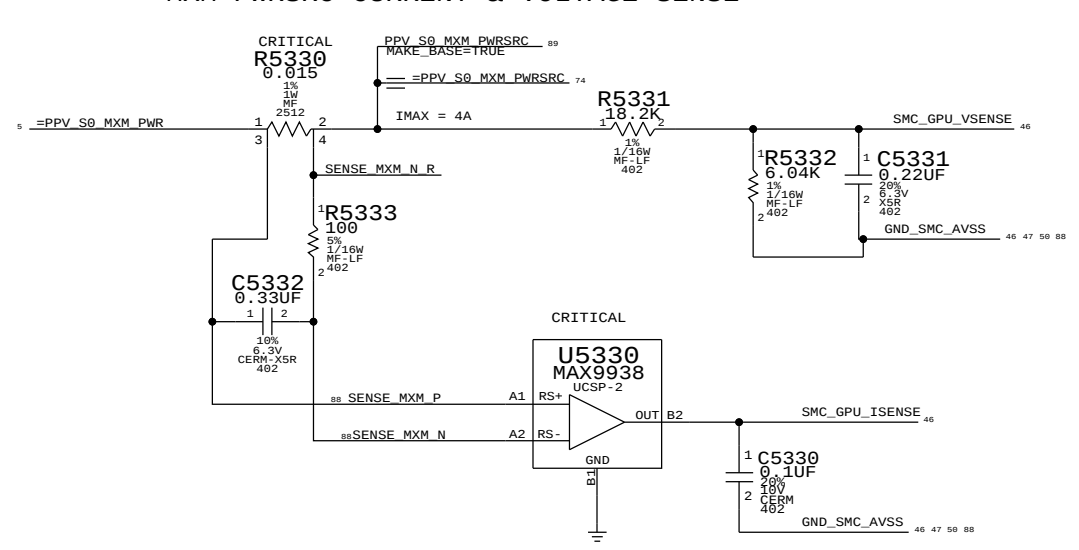
CPU CURRENT SENSE AMP & FILTER



CPU VTT CURRENT SENSE



MXM PWRSRC CURRENT & VOLTAGE SENSE



SYNC MASTER=K74 MASTER

SYNC DATE=N/A

CPU/GPU POWER SENSE

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051-8337

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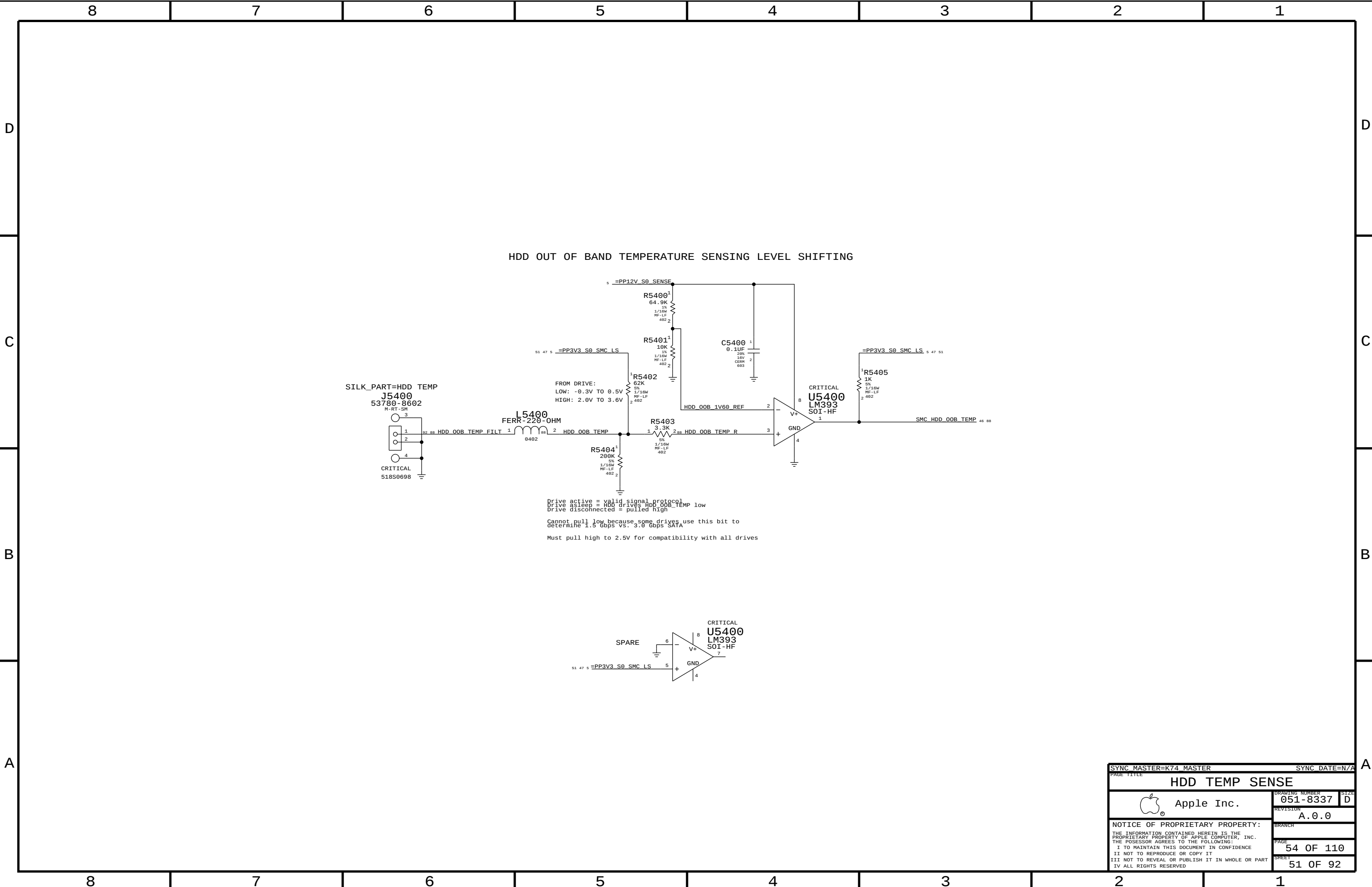
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D



B

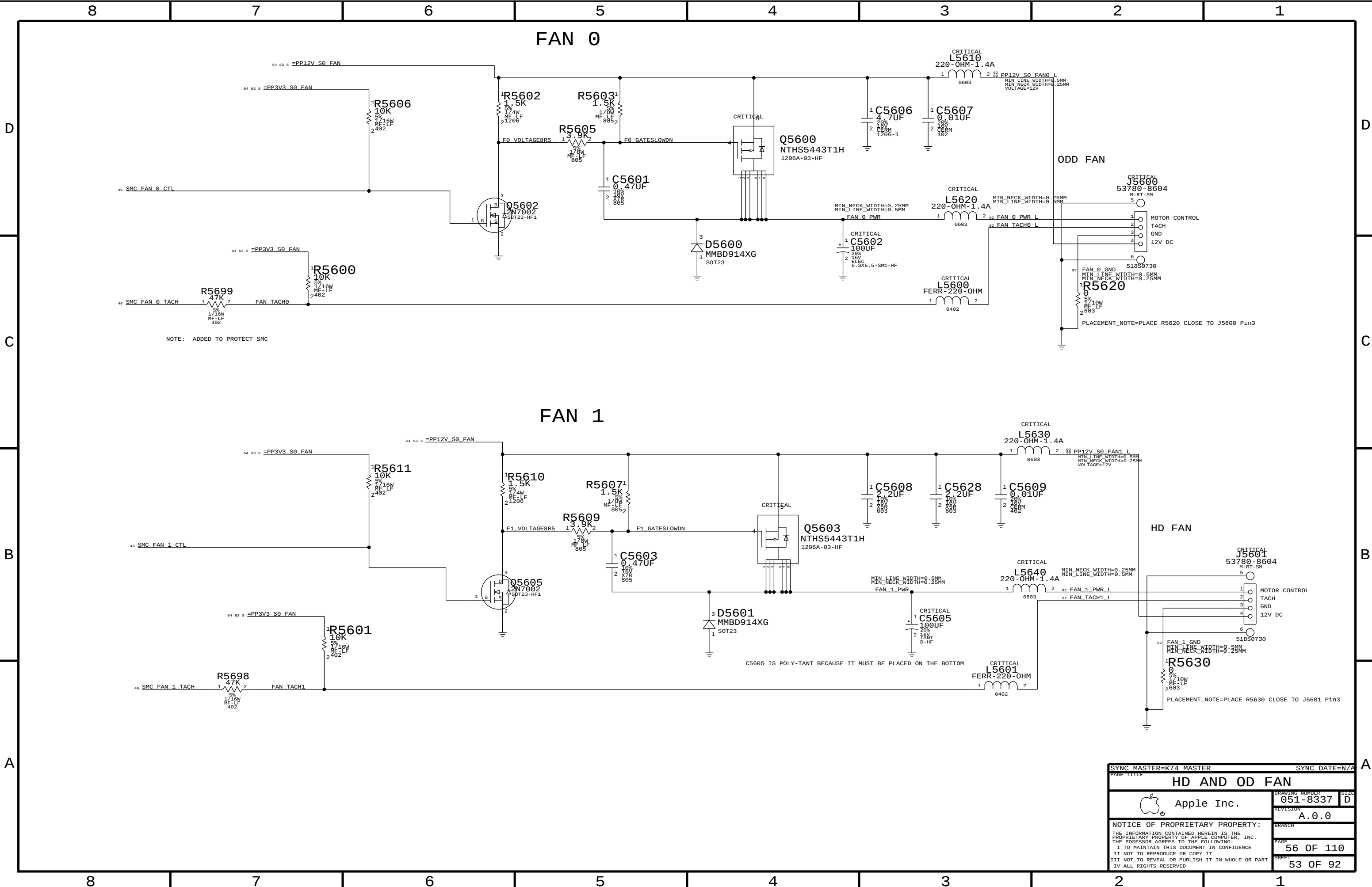


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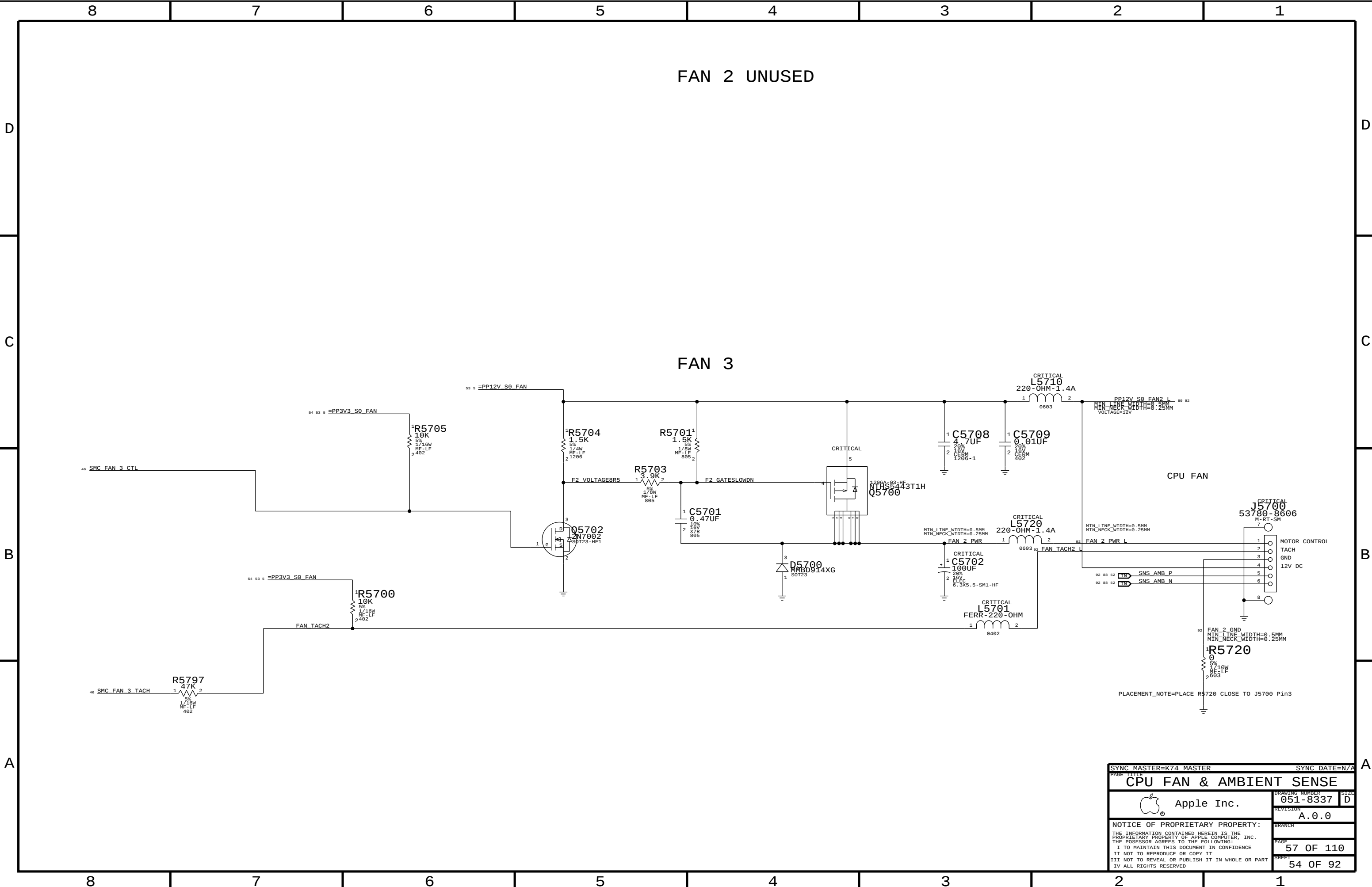
NOTE: ADDED TO PROTECT SMC

C5605 IS POLY-TANT BECAUSE IT MUST BE PLACED ON THE BOTTOM

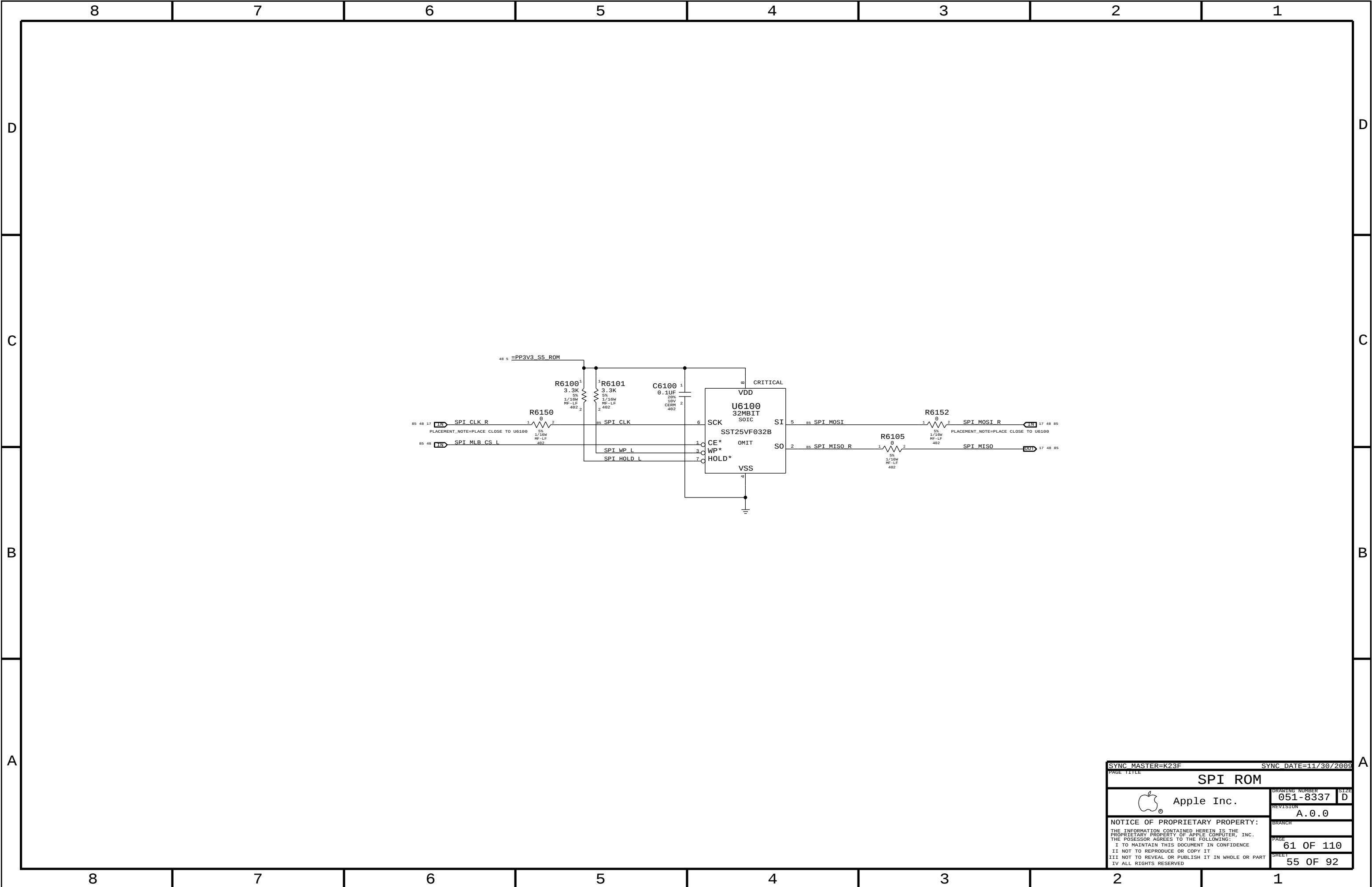
PLACEMENT_NOTE=PLACE R5620 CLOSE TO J5600 Pin3

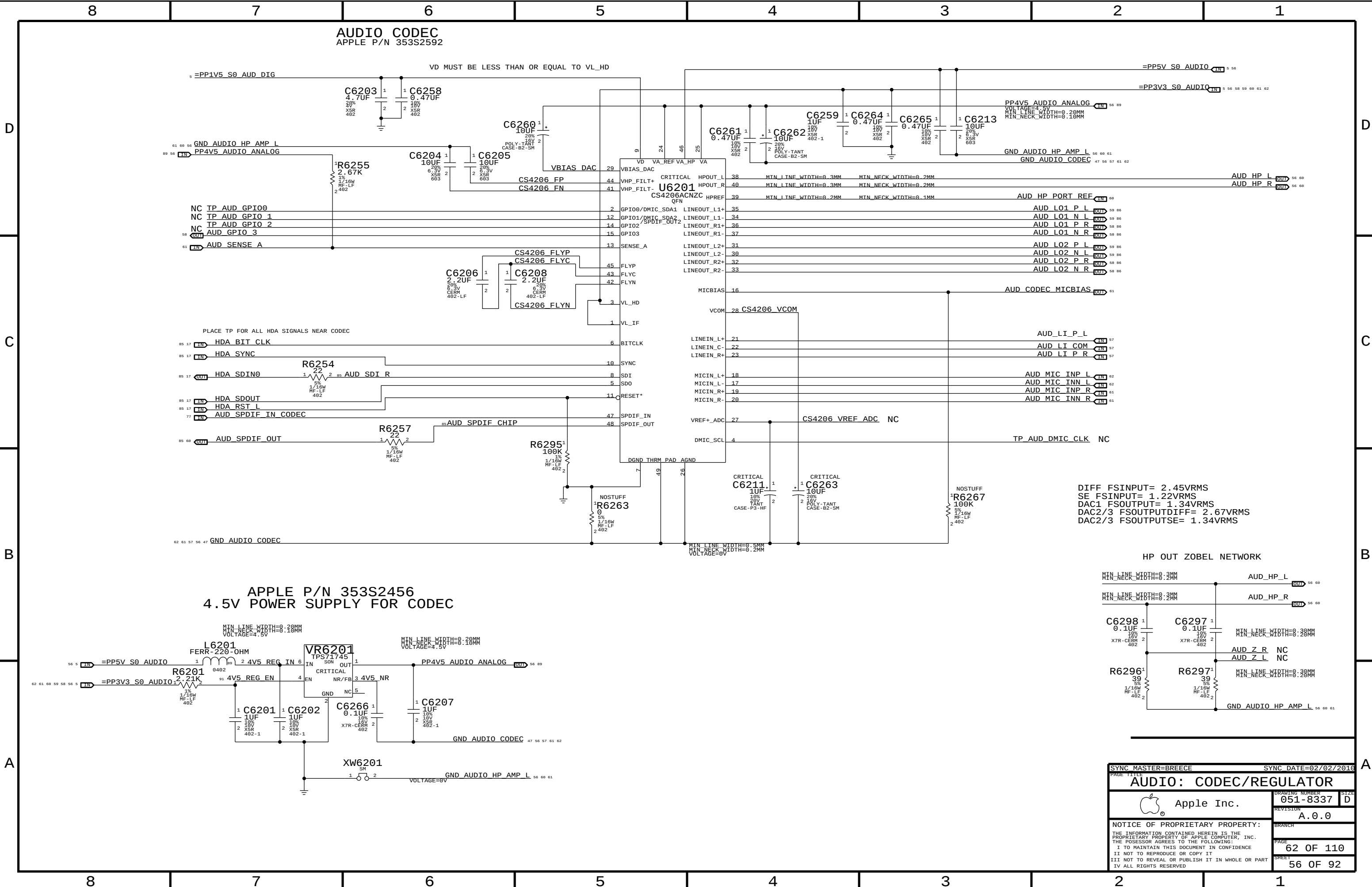
PLACEMENT_NOTE=PLACE R5630 CLOSE TO J5601 Pin3

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
HD AND OD FAN			
 Apple Inc.	DRAWING NUMBER		SIZE
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		REVISION	
		A.0.0	
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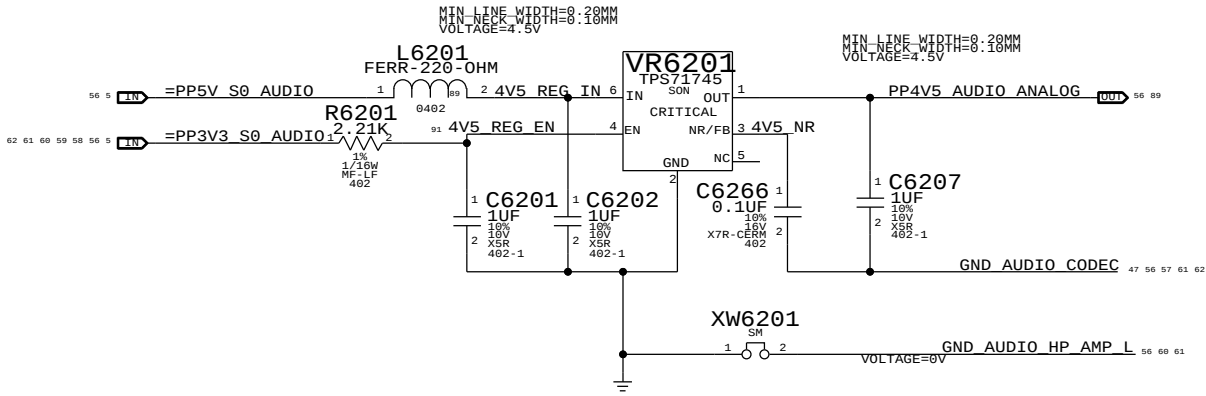


SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE		CPU FAN & AMBIENT SENSE	
DRAWING NUMBER		051-8337	SIZE D
REVISION		A.0.0	BRANCH
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		SHEET	54 OF 92



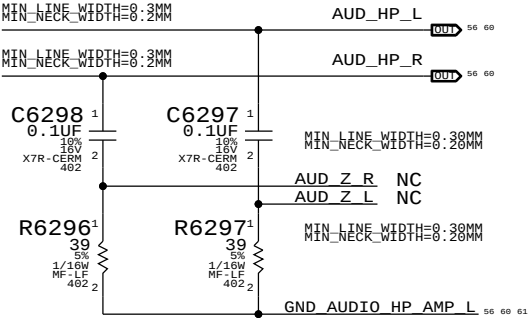


APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

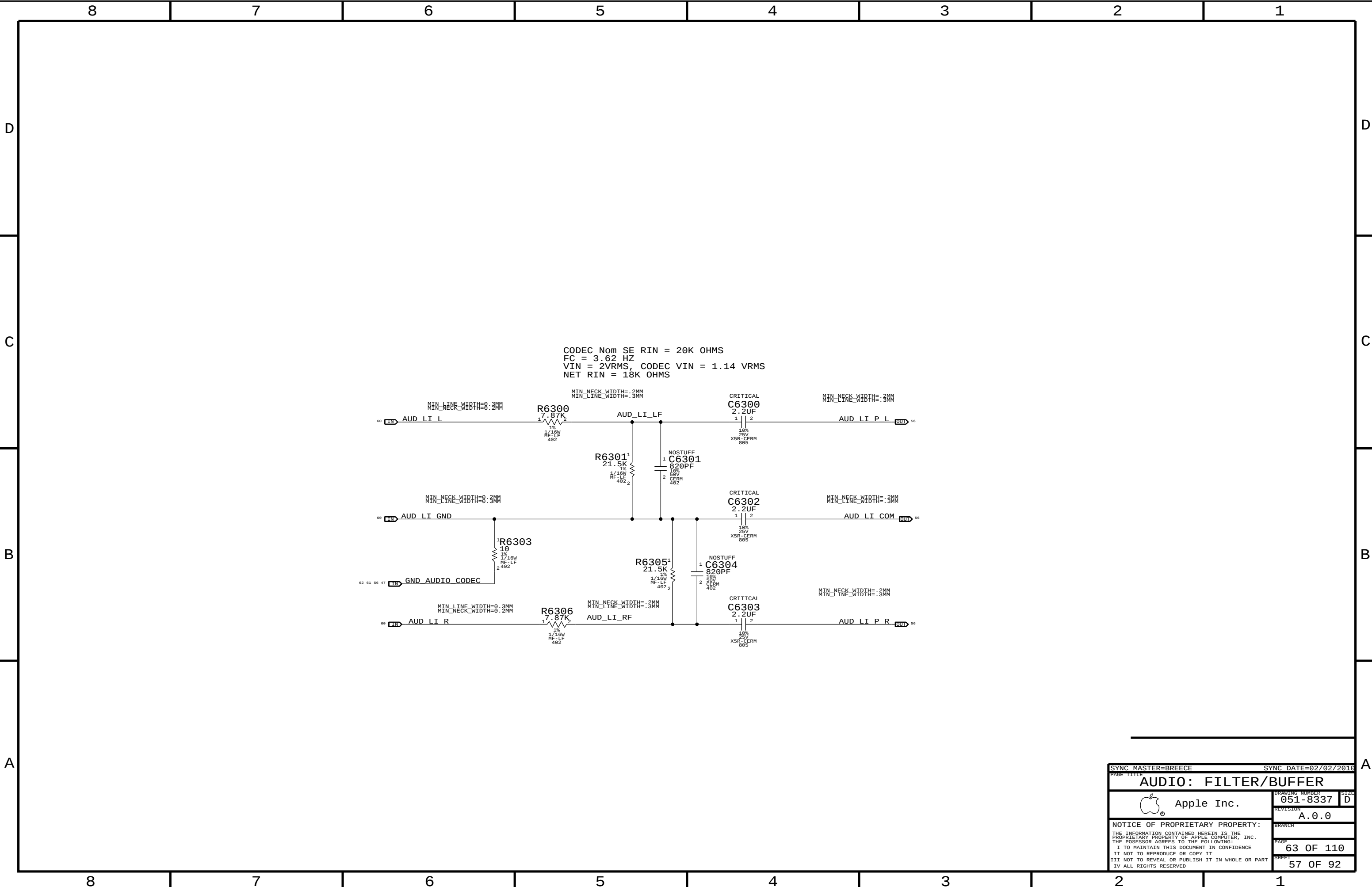


DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

HP OUT ZOBEL NETWORK



PAGE TITLE		SYNC DATE=02/02/2016	
AUDIO: CODEC/REGULATOR		DRAWING NUMBER	051-8337
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		PAGE	62 OF 110
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SYNC MASTER=BREECE

SYNC DATE=02/02/2016

AUDIO: FILTER/BUFFER

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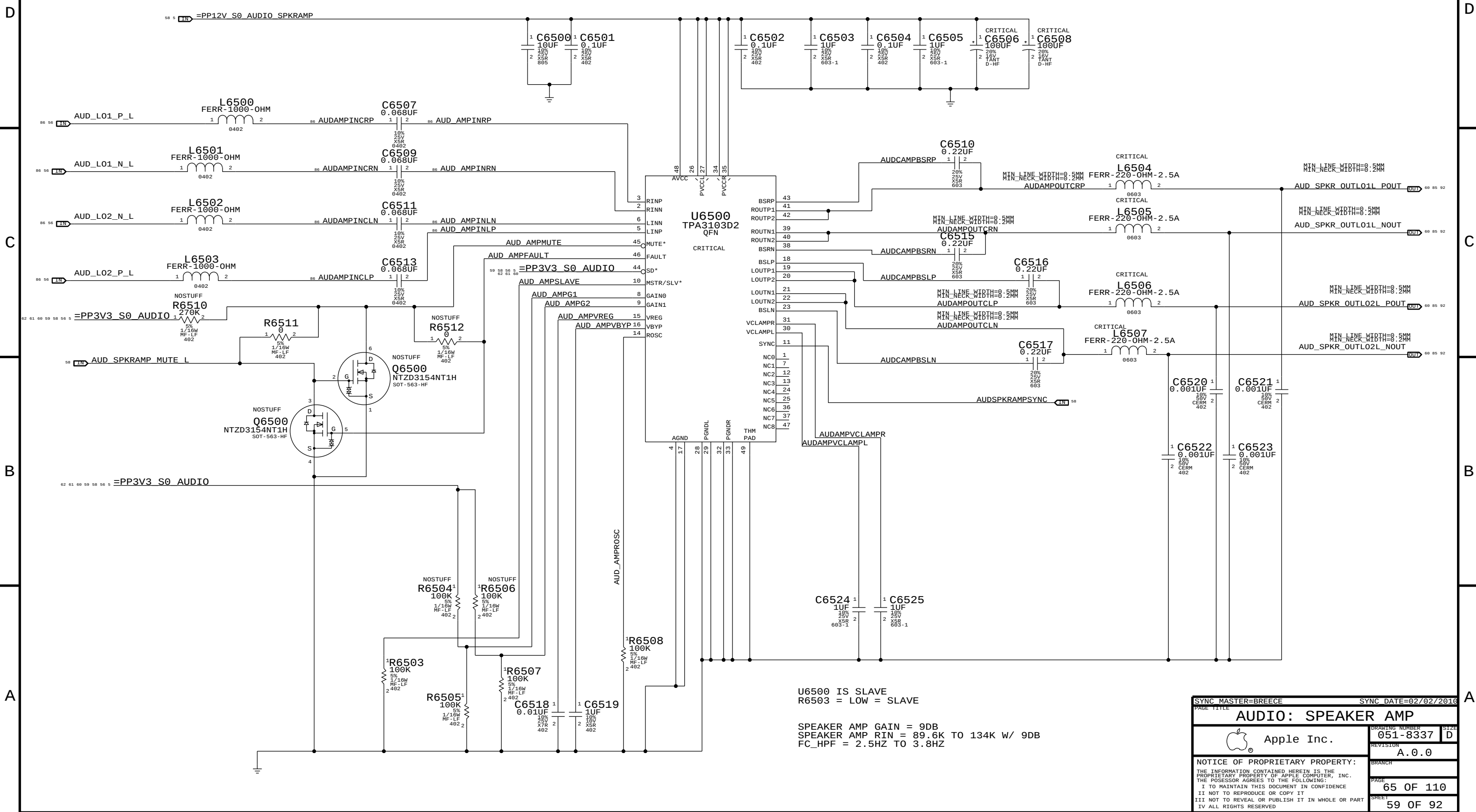
B

A

B

A

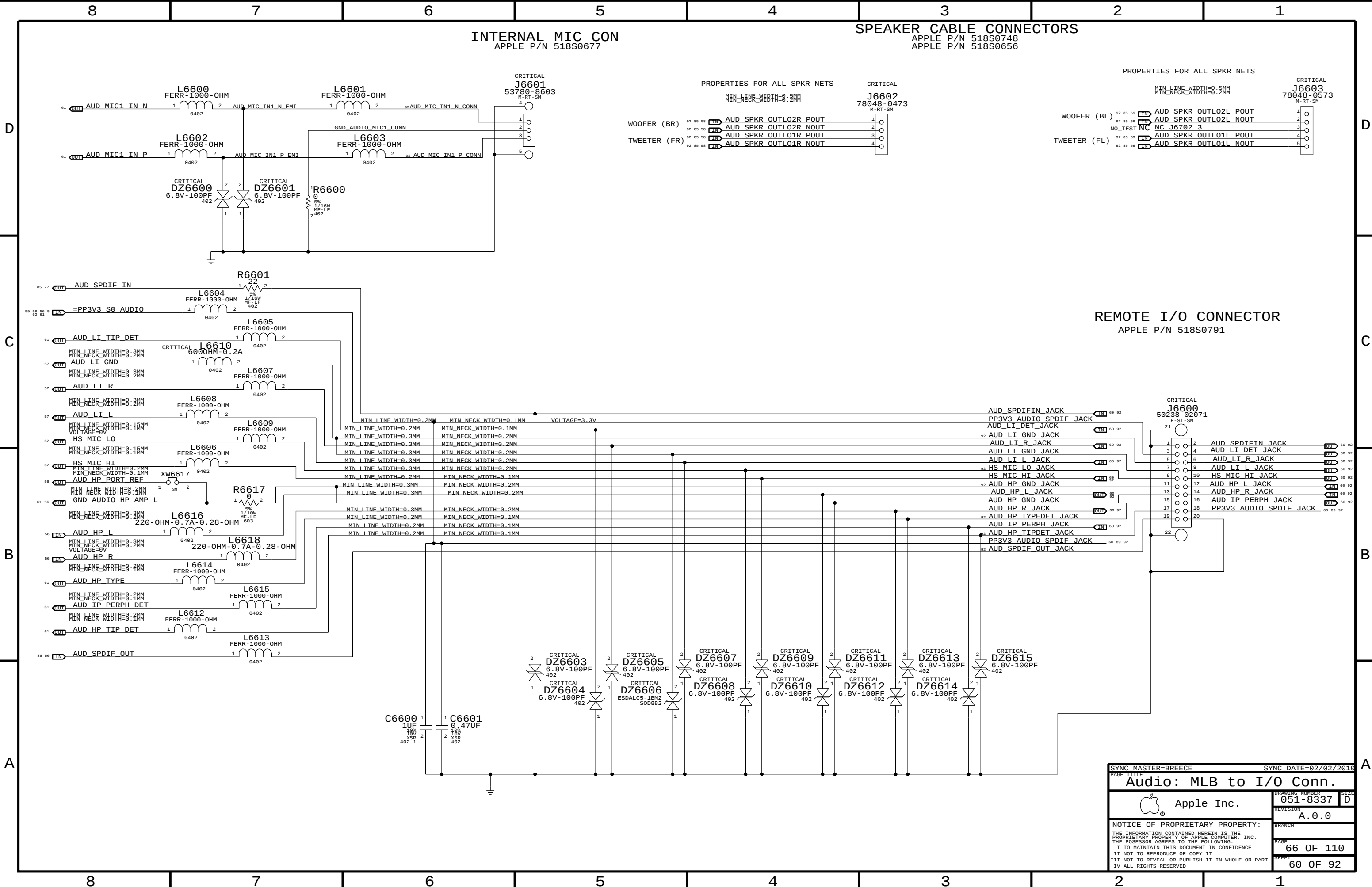
LEFT CH. SPEAKER AMP
APPLE P/N 353S2768



U6500 IS SLAVE
R6503 = LOW = SLAVE

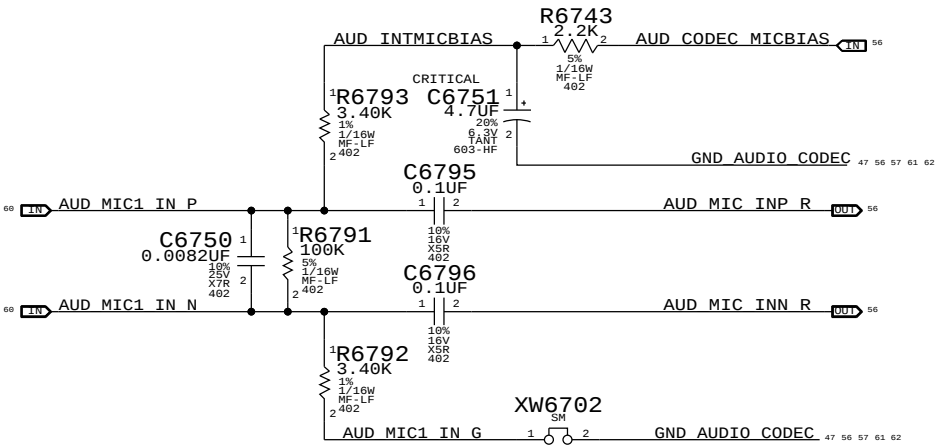
SPEAKER AMP GAIN = 9DB
SPEAKER AMP RIN = 89.6K TO 134K W/ 9DB
FC_HPF = 2.5HZ TO 3.8HZ

PAGE TITLE		SYNC DATE=02/02/2016	
AUDIO: SPEAKER AMP		DRAWING NUMBER	051-8337
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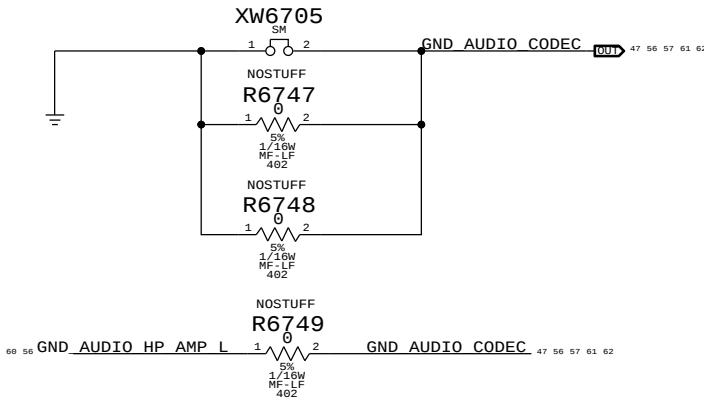


SYNC MASTER=BREECE		SYNC DATE=02/02/2016	
PAGE TITLE		Audio: MLB to I/O Conn.	
Apple Inc.		DRAWING NUMBER	051-8337
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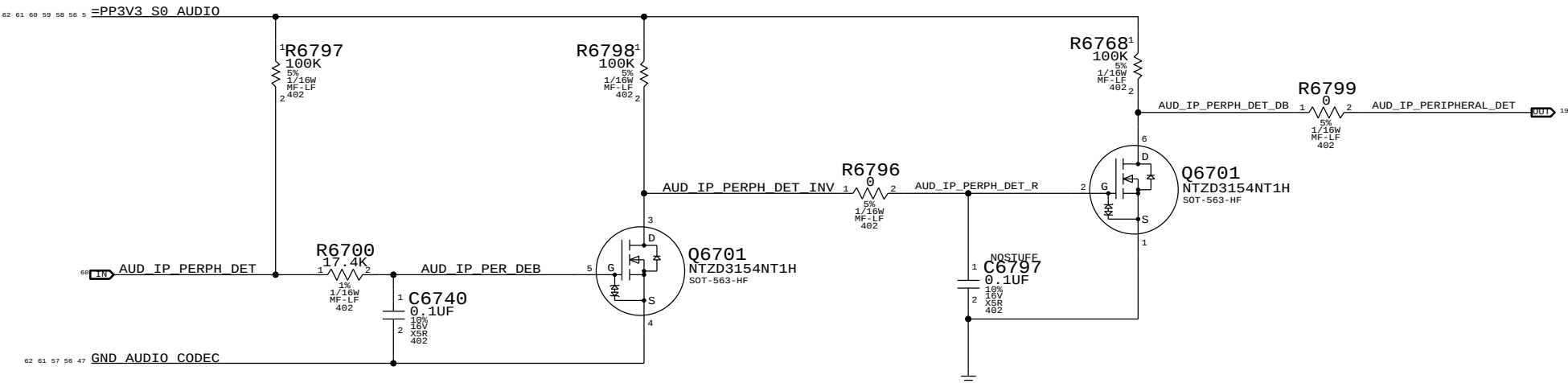
Internal Microphone Impedance Matching



AUDIO STAR GND AND STUFFING OPTIONS



IPHS HS Detect Debounce CKT

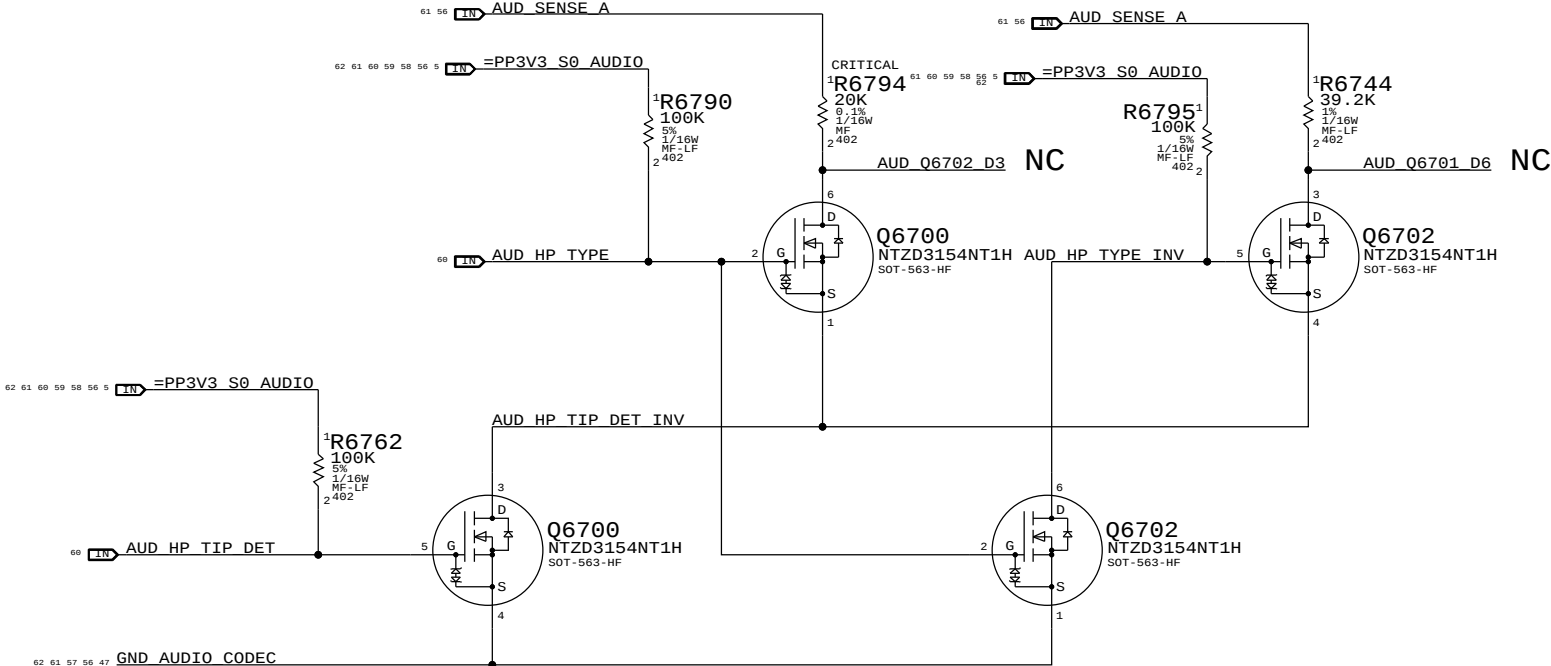


Digital Out

Headphone Out

LI Insert Detect

DP Audio Enable

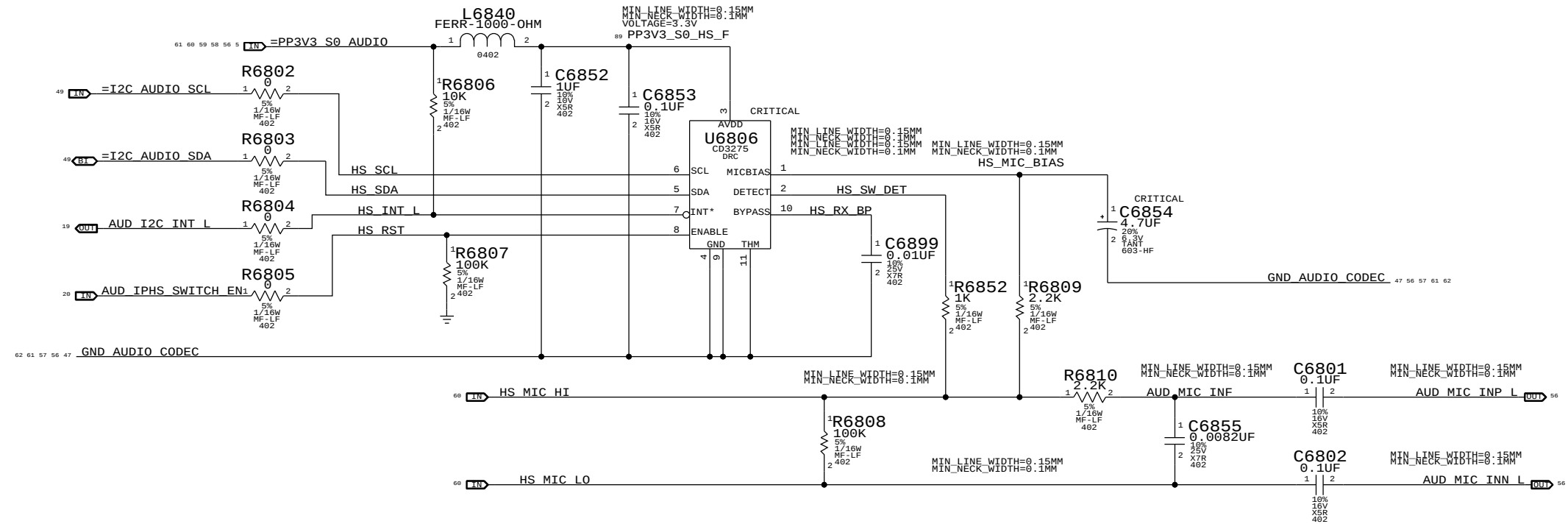


SYNC MASTER=BREECE		SYNC DATE=02/02/2016	
PAGE TITLE		AUDIO: Detects/Grounding	
Apple Inc.		DRAWING NUMBER	051-8337
		REVISION	A.0.0
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FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0D (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5

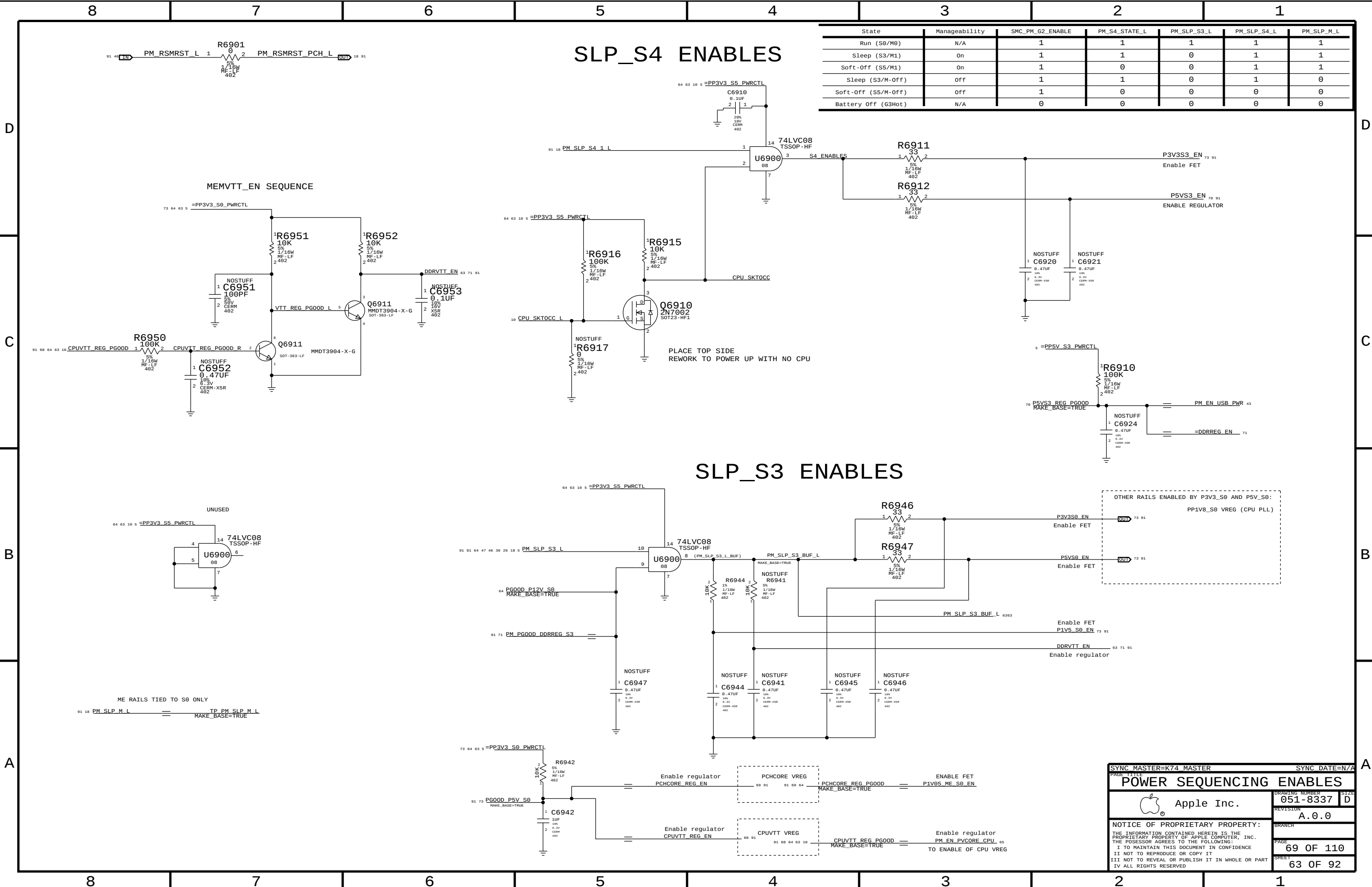
MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256



FLP = 8.82 KHZ
FHP = 80 HZ

PAGE TITLE		SYNC MASTER=BREECE		SYNC DATE=02/02/2016	
AUDIO: Mikey		DRAWING NUMBER		SIZE	
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SLP_S4 ENABLES

State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SLP_S3 ENABLES

SYNC MASTER=K74 MASTER

SYNC DATE=N/A

POWER SEQUENCING ENABLES

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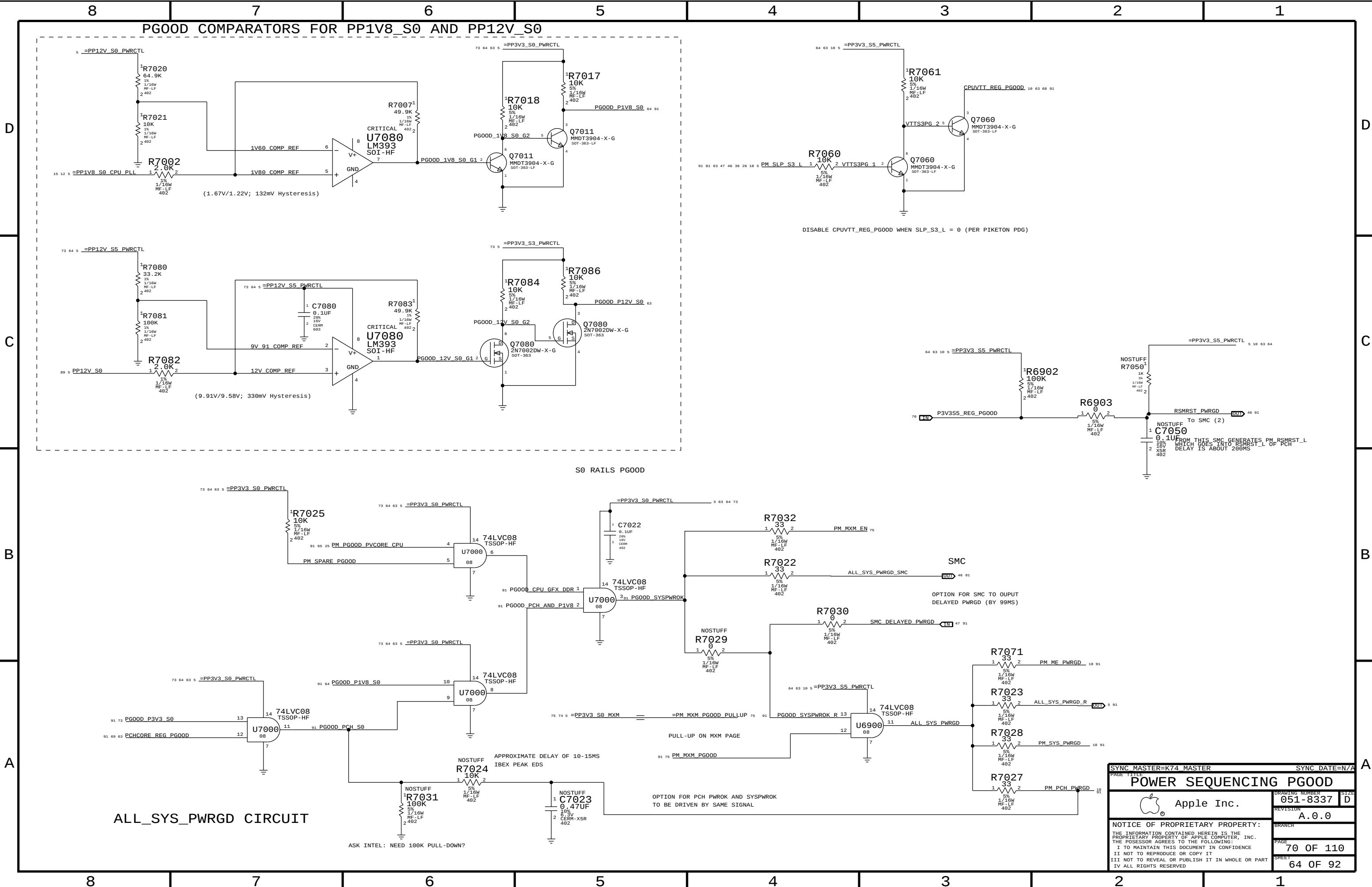
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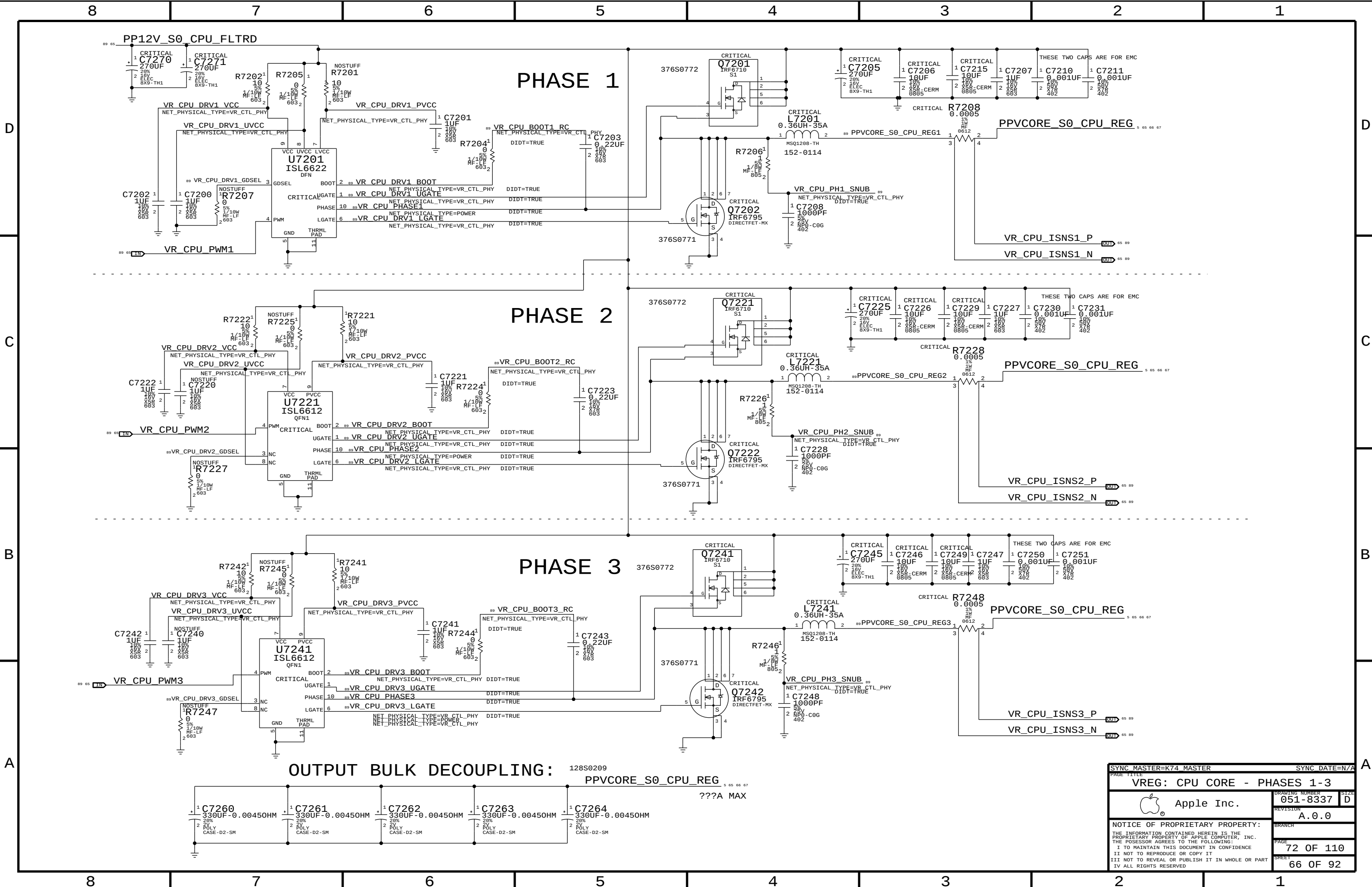
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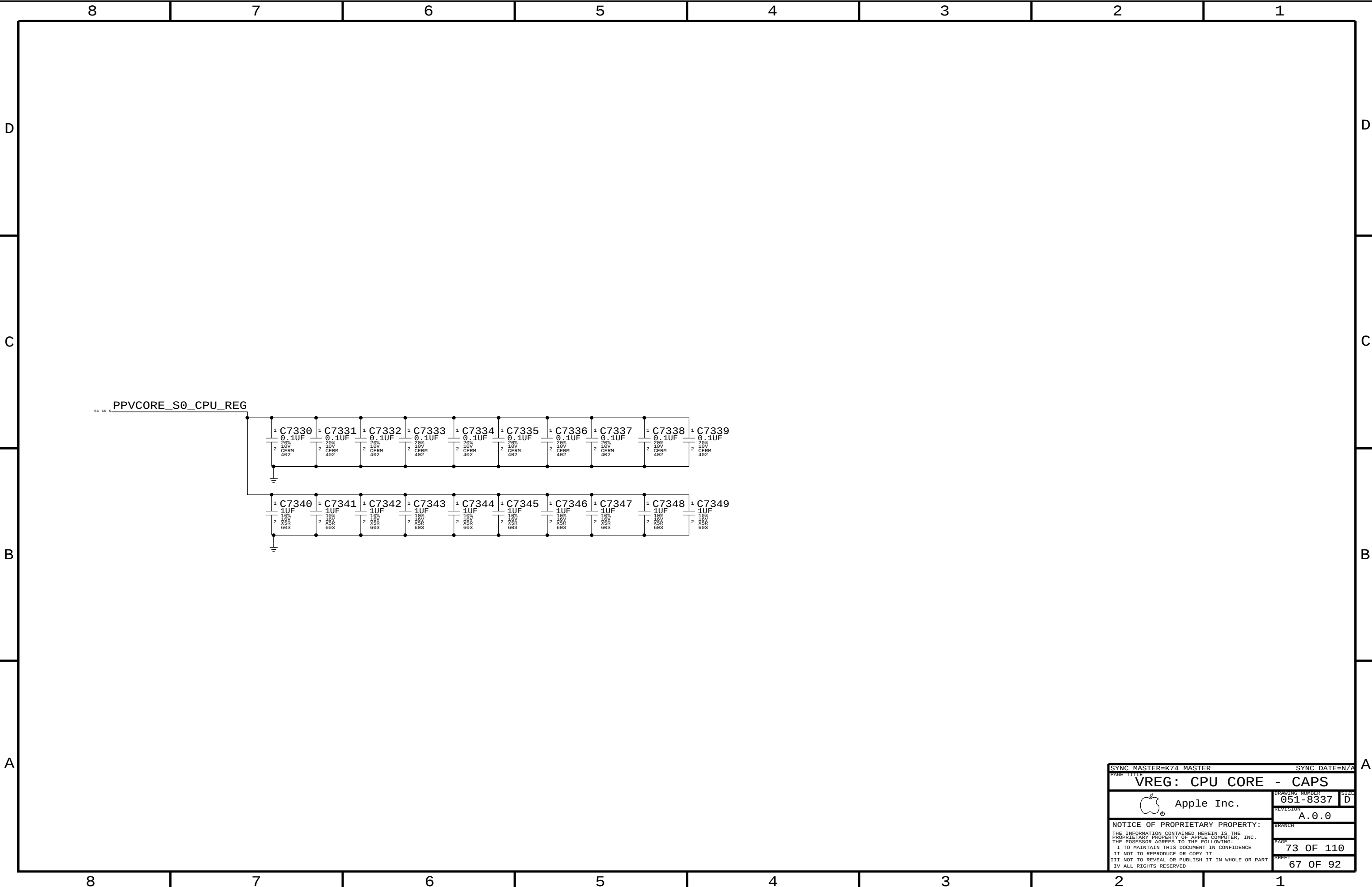
ALL_SYS_PWRGD CIRCUIT

PAGE TITLE		SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
POWER SEQUENCING PG00D		DRAWING NUMBER		SIZE	
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		PAGE		SHEET	
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OUTPUT BULK DECOUPLING: 128S0209
PPVCORE_S0_CPU_REG 5 65 66 67
???A MAX

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE		VREG: CPU CORE - PHASES 1-3	
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		REVISION	A.0.0
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SYNC MASTER=K74 MASTER

SYNC DATE=N/A

VREG: CPU CORE - CAPS

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DRAWING NUMBER

051-8337

SIZE

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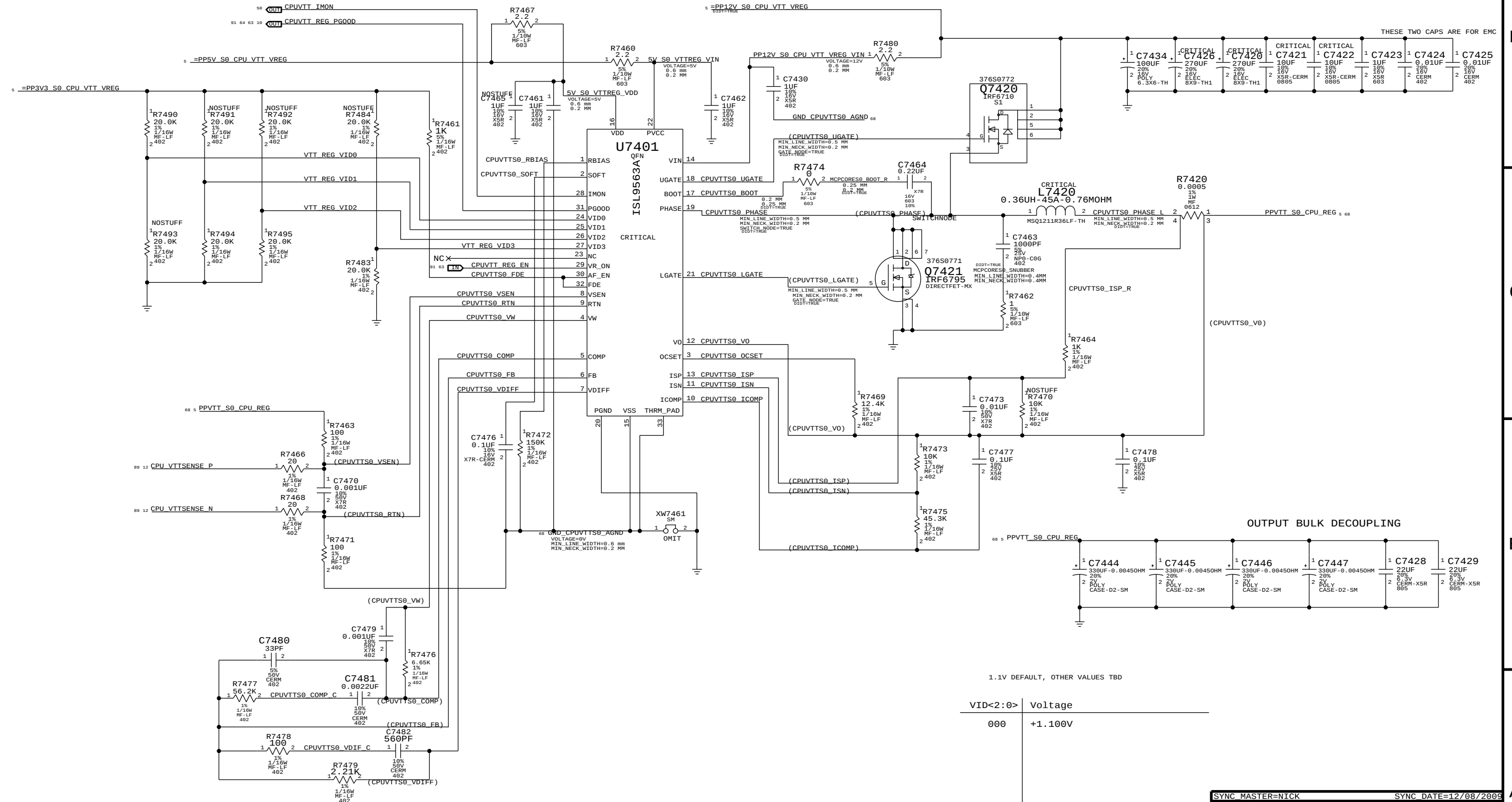
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CPU VTT REG 1.1V

0/P= PPVTT_S0_CPU_REG



1.1V DEFAULT, OTHER VALUES TBD

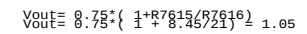
VID<2:0>	Voltage
000	+1.100V

SYNC MASTER-NICK		SYNC DATE=12/08/2009	
PAGE TITLE			
CPU VTT REGULATOR			
 Apple Inc.		DRAWING NUMBER	SIZE
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		BRANCH	
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IBEX PEAK CORE REG 1.05V OUTPUT = PP1V05_S0_REG

PP1V05_S0_REG
VOUT = 1.05V
PEAK = 7.5A
AVG = 3A

$$AVG = 3A$$


SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
IBEX PEAK CORE			
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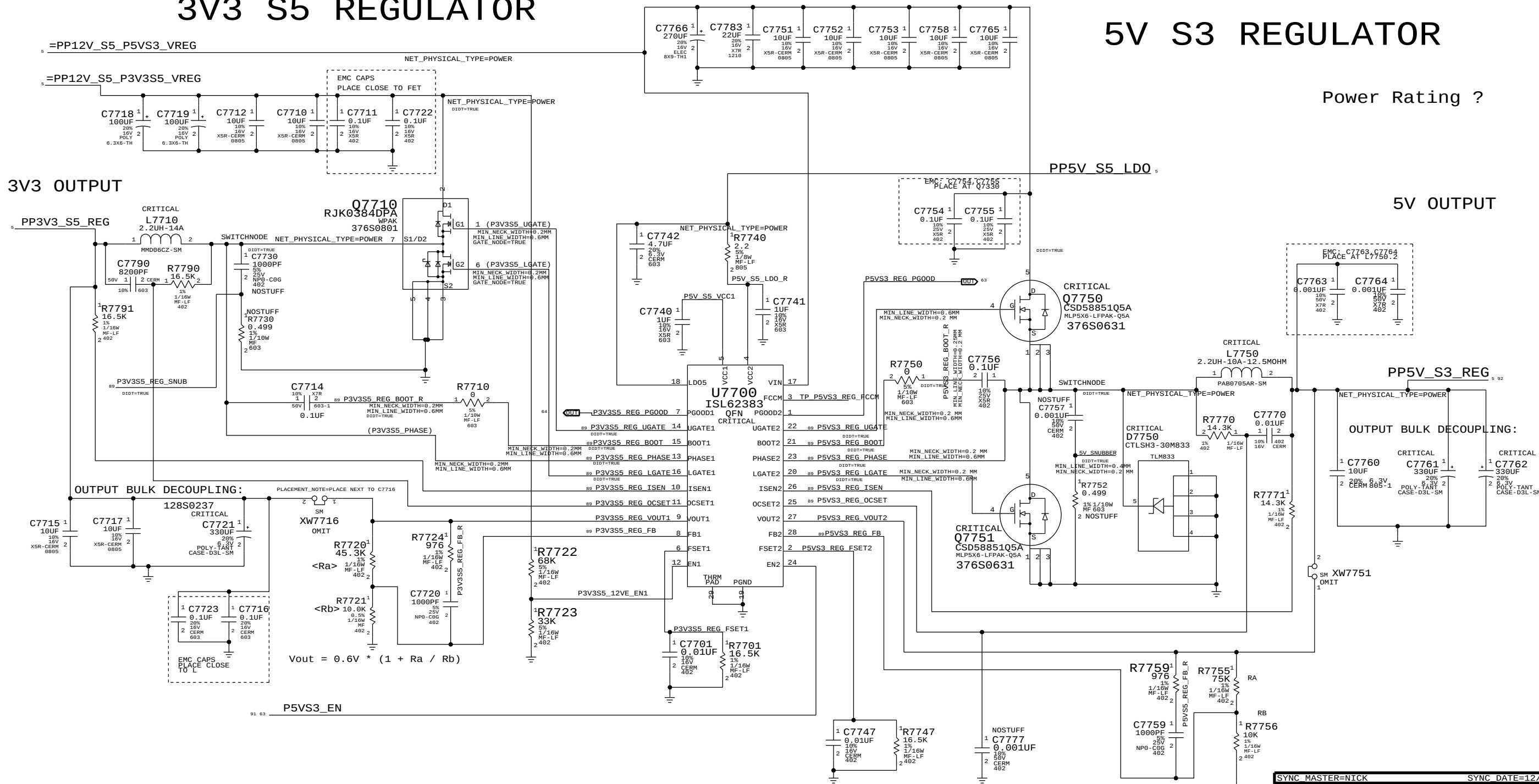
3V3 S5 REGULATOR

5V S3 REGULATOR

Power Rating ?

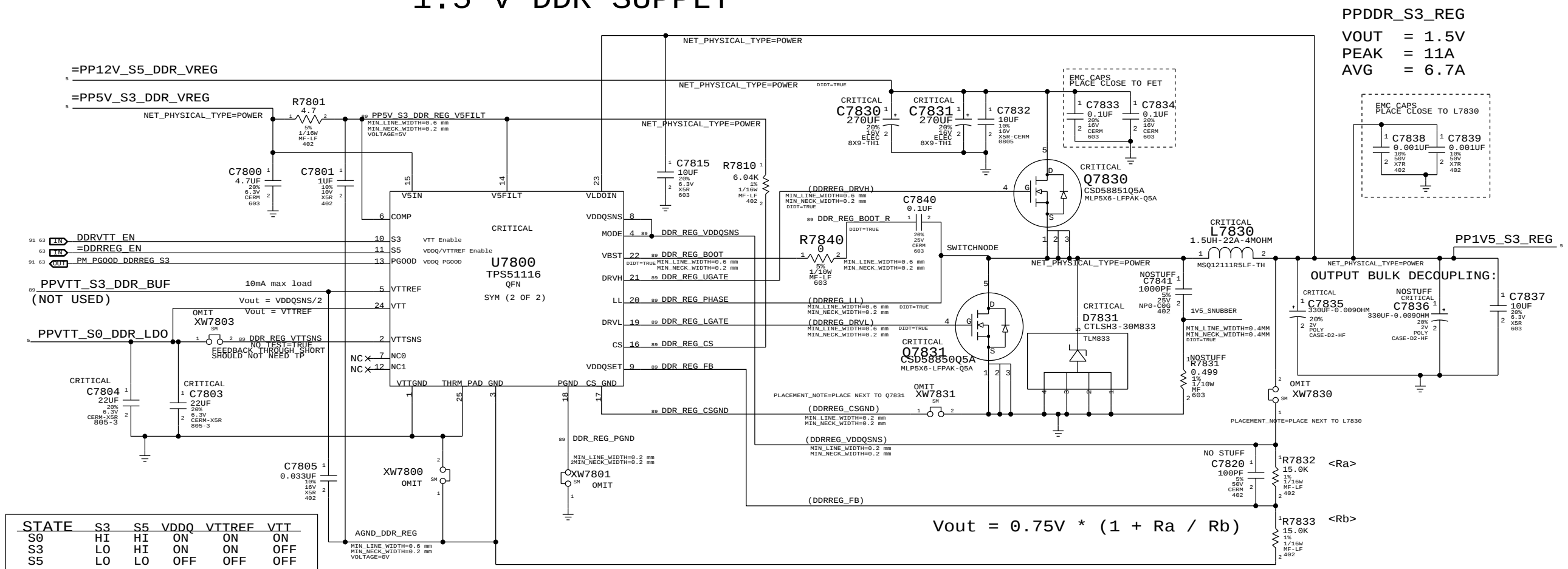
5V OUTPUT

3V3 OUTPUT

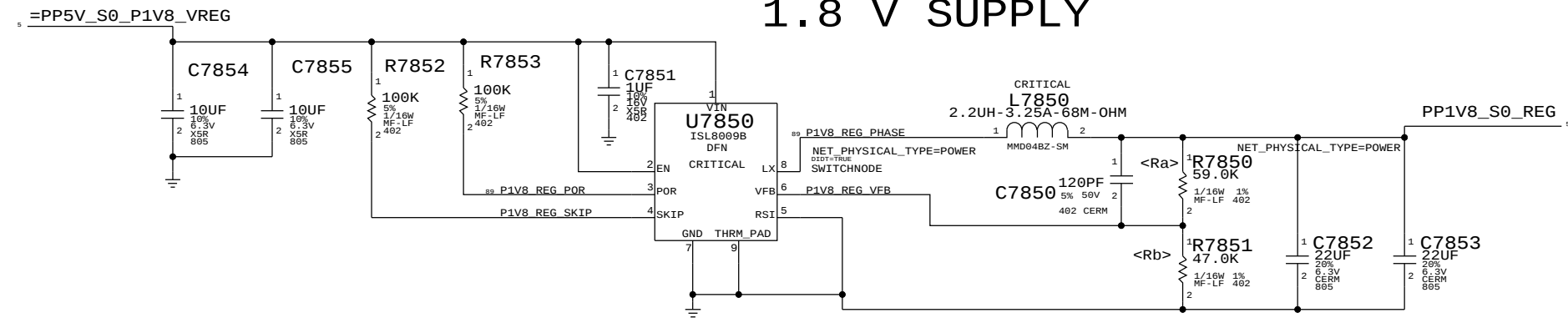


PAGE TITLE		PAGE TITLE	
5V_S3 / 3V3_S5 VREGS		5V_S3 / 3V3_S5 VREGS	
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051-8337		051-8337	
REVISION		REVISION	
A.0.0		A.0.0	
BRANCH		BRANCH	
77 OF 110		77 OF 110	
SHEET		SHEET	
70 OF 92		70 OF 92	

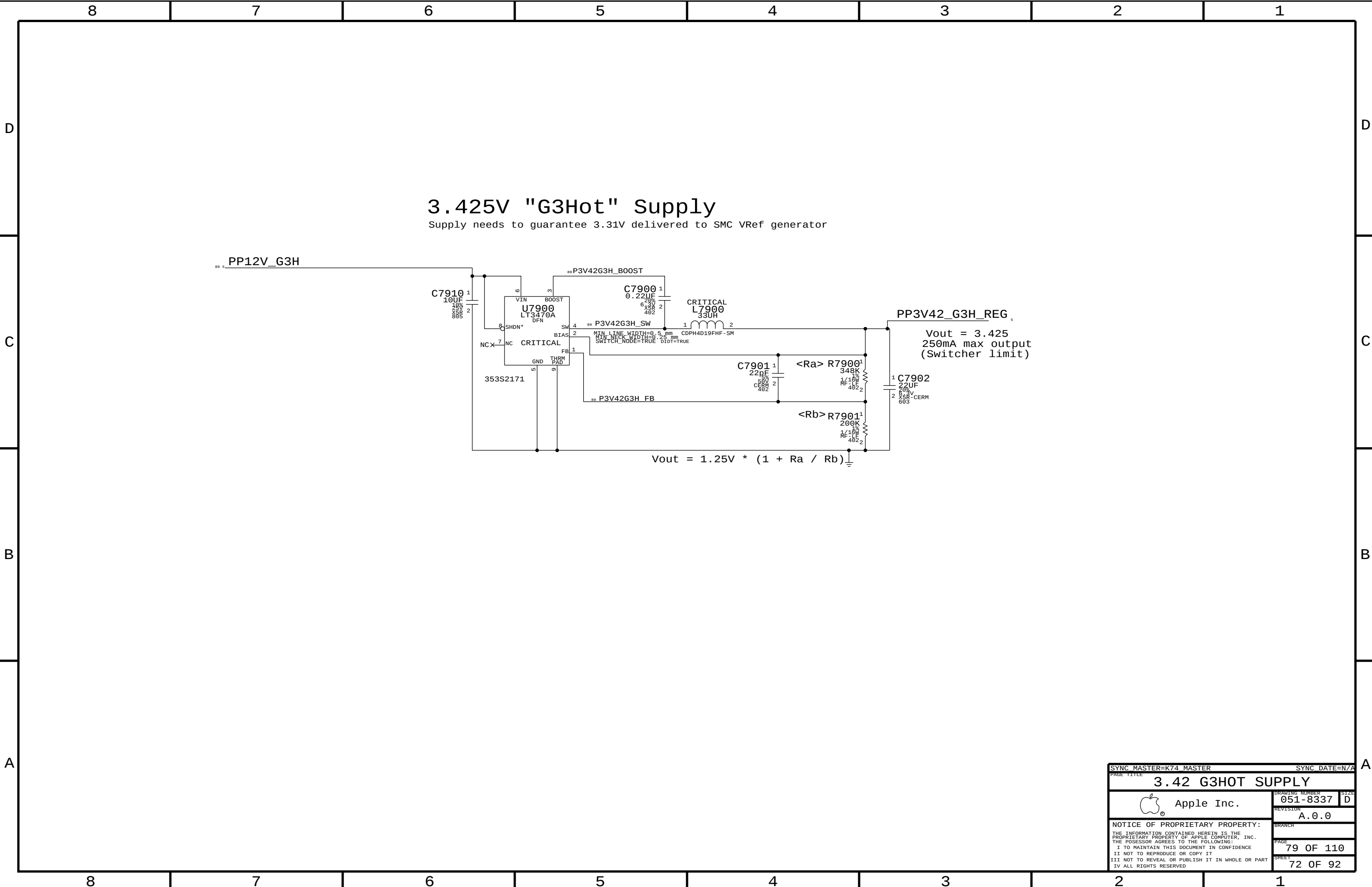
1.5 V DDR SUPPLY

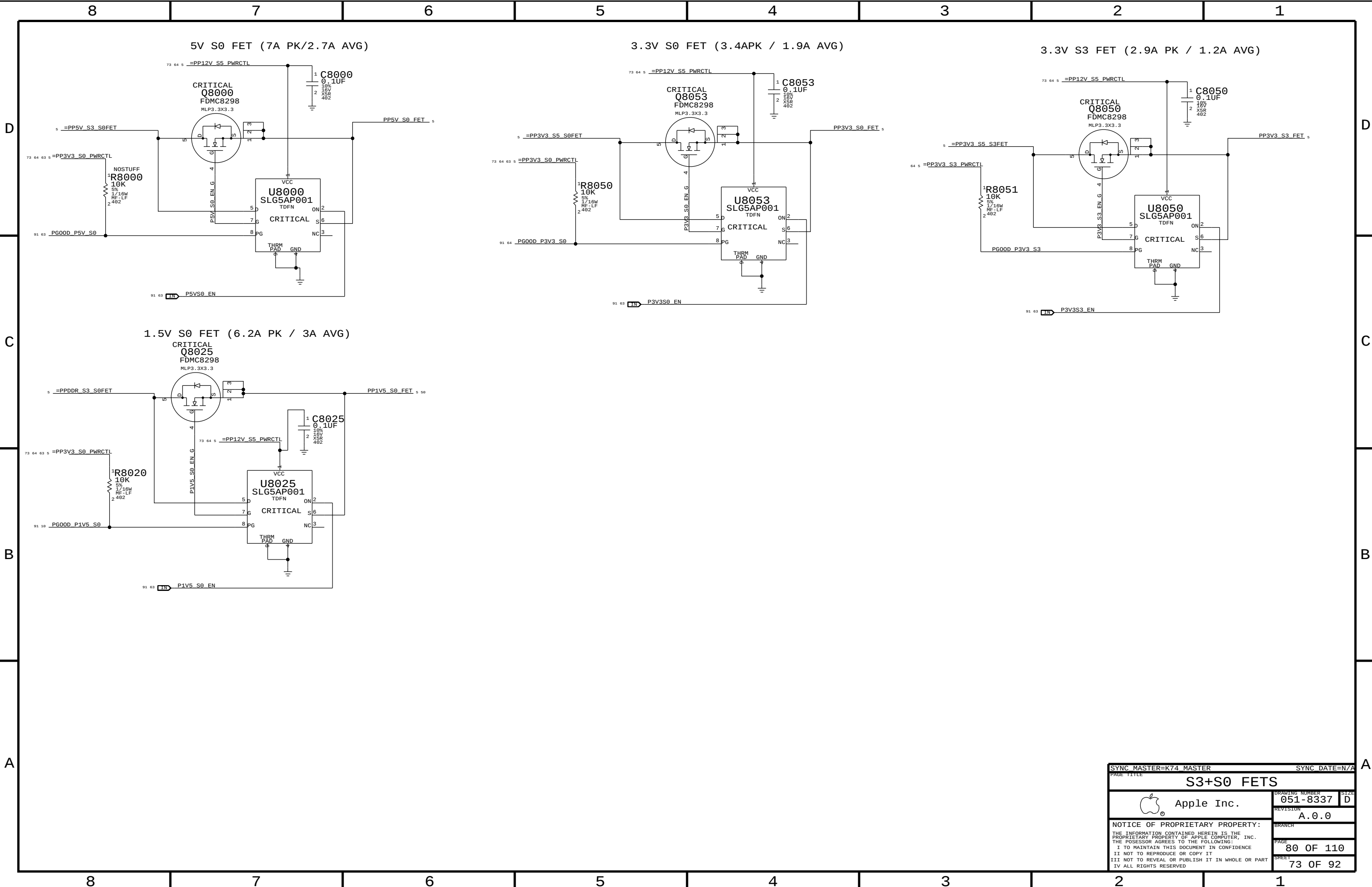


1.8 V SUPPLY



SYNC MASTER=K23F		SYNC DATE=11/30/2009	
PAGE TITLE		1.5V / 1.8V VREGS	
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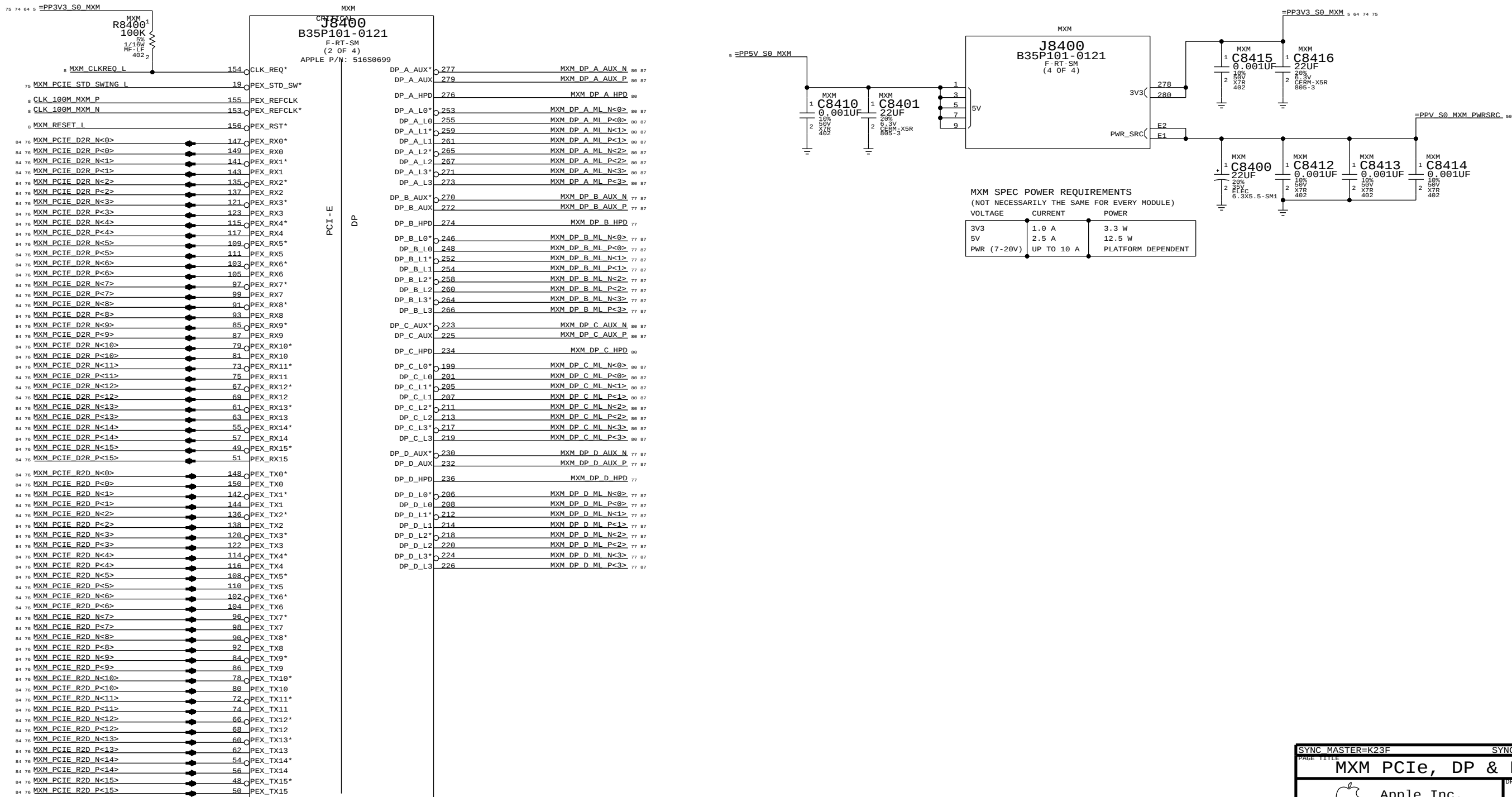
Power aliases required by this page:

- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

- MXM



SYNC MASTER=K23F		SYNC DATE=11/30/2009	
PAGE TITLE			
MXM PCIe, DP & Power			
Apple Inc.		DRAWING NUMBER	051-8337
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		PAGE	84 OF 110
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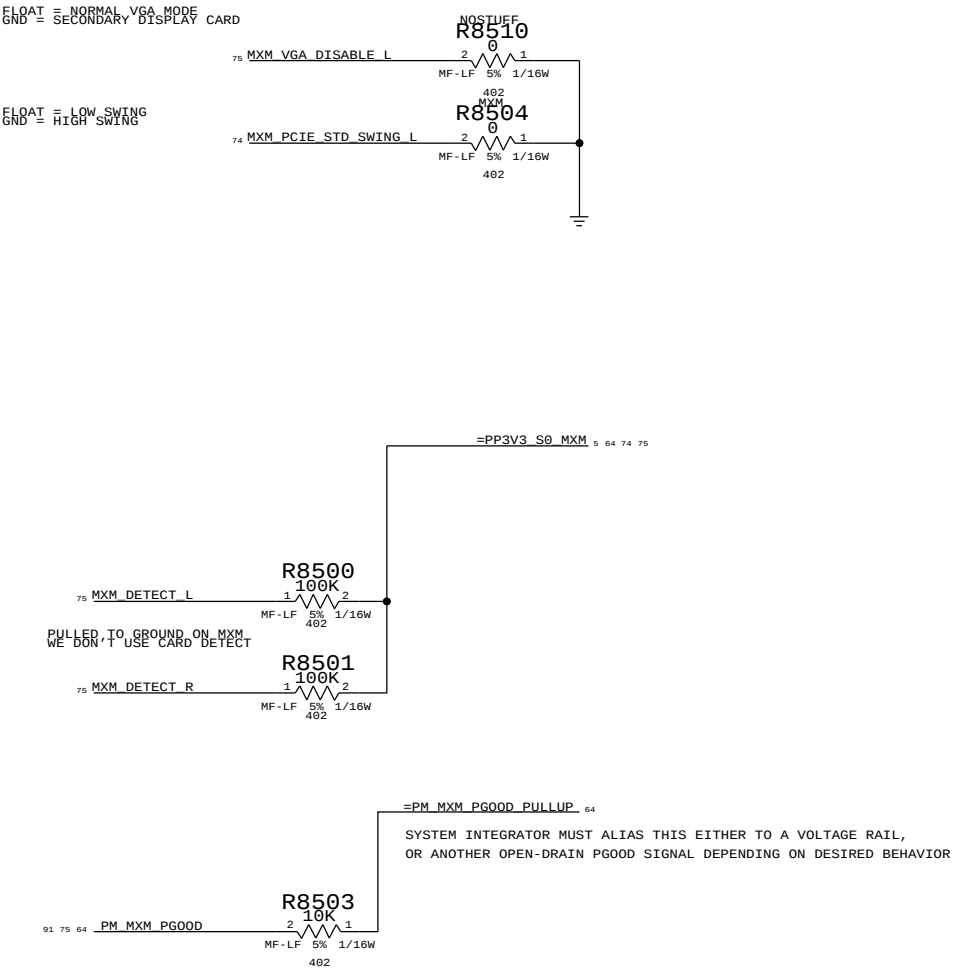
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA - =PM_MXM_PG00D_PULLUP
- =SMB_MXM_THRM_CLK

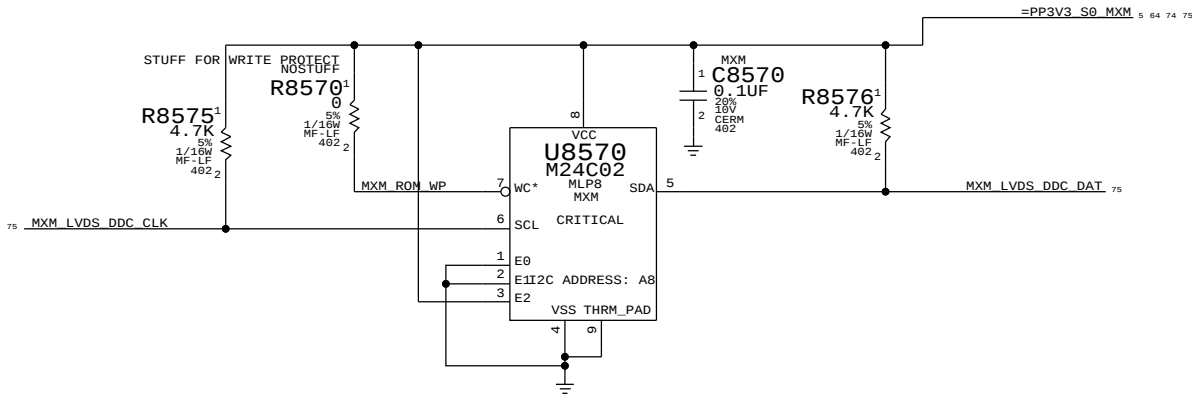
BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR



MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



PAGE TITLE		SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
MXM I/O		DRAWING NUMBER		SIZE	
Apple Inc.		051-8337		D	
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Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Unused MXM Interfaces

87 75	MXM LVDS A CLK N	==	NC MXM LVDS A CLK N	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS A CLK P	==	NC MXM LVDS A CLK P	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS A DATA N<0>	==	NC MXM LVDS A DATA N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS A DATA P<0>	==	NC MXM LVDS A DATA P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS A DATA N<1>	==	NC MXM LVDS A DATA N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS A DATA P<1>	==	NC MXM LVDS A DATA P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS A DATA N<2>	==	NC MXM LVDS A DATA N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS A DATA P<2>	==	NC MXM LVDS A DATA P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS A DATA N<3>	==	NC MXM LVDS A DATA N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS A DATA P<3>	==	NC MXM LVDS A DATA P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS B CLK N	==	NC MXM LVDS B CLK N	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS B CLK P	==	NC MXM LVDS B CLK P	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS B DATA N<0>	==	NC MXM LVDS B DATA N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS B DATA P<0>	==	NC MXM LVDS B DATA P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS B DATA N<1>	==	NC MXM LVDS B DATA N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS B DATA P<1>	==	NC MXM LVDS B DATA P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS B DATA N<2>	==	NC MXM LVDS B DATA N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS B DATA P<2>	==	NC MXM LVDS B DATA P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS B DATA N<3>	==	NC MXM LVDS B DATA N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 75	MXM LVDS B DATA P<3>	==	NC MXM LVDS B DATA P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE

Unused MXM DP Interfaces

87 74	MXM DP B MI P<0..3>	==	NC MXM DP B MI P<0..3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM DP B MI N<0..3>	==	NC MXM DP B MI N<0..3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM DP B AUX P	==	NC MXM DP B AUX P	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM DP B AUX N	==	NC MXM DP B AUX N	MAKE_BASE=TRUE	NO_TEST=TRUE
74	MXM DP B HPD	==	NC MXM DP B HPD	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM DP D MI P<0..3>	==	NC MXM DP D MI P<0..3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM DP D MI N<0..3>	==	NC MXM DP D MI N<0..3>	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM DP D AUX P	==	NC MXM DP D AUX P	MAKE_BASE=TRUE	NO_TEST=TRUE
87 74	MXM DP D AUX N	==	NC MXM DP D AUX N	MAKE_BASE=TRUE	NO_TEST=TRUE
74	MXM DP D HPD	==	NC MXM DP D HPD	MAKE_BASE=TRUE	NO_TEST=TRUE

UNUSED MXM CONTROL SIGNALS

75	MXM PNL BL EN	==	NC MXM PNL BL EN	MAKE_BASE=TRUE	NO_TEST=TRUE
75	MXM PNL PWR EN	==	NC MXM PNL PWR EN	MAKE_BASE=TRUE	NO_TEST=TRUE

DISPLAY AUDIO MUX NOT USED - SEND SPDIF TO CODEC

85 60	TPN	AUD SPDIF IN	==	AUD SPDIF IN CODEC	OUT	56
		MAKE_BASE=TRUE				
78	TPN	DP INT SPDIF AUDIO	==	TP DP INT SPDIF AUDIO		
		MAKE_BASE=TRUE				

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
Display: Aliases			
 Apple Inc.		DRAWING NUMBER	051-8337
		SIZE	D
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		PAGE	87 OF 110
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Power aliases required by this page:

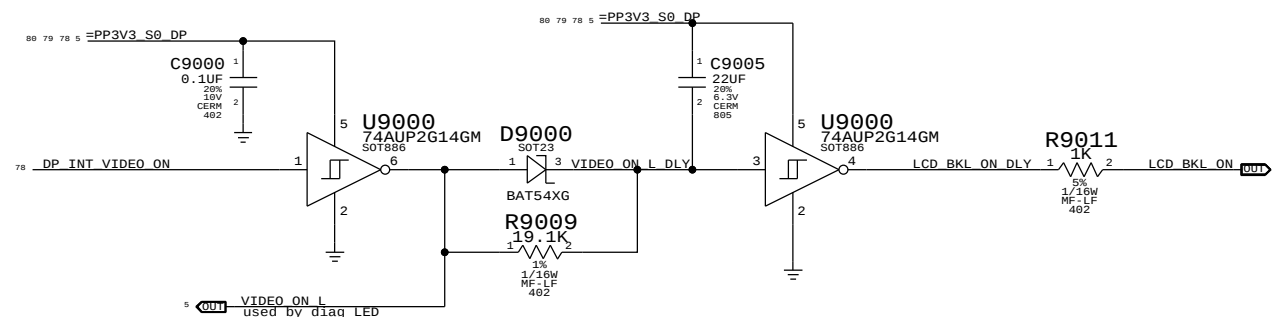
- =PP12V_S0_LCD
- =PP3V3_S0_DP

Signal aliases required by this page:

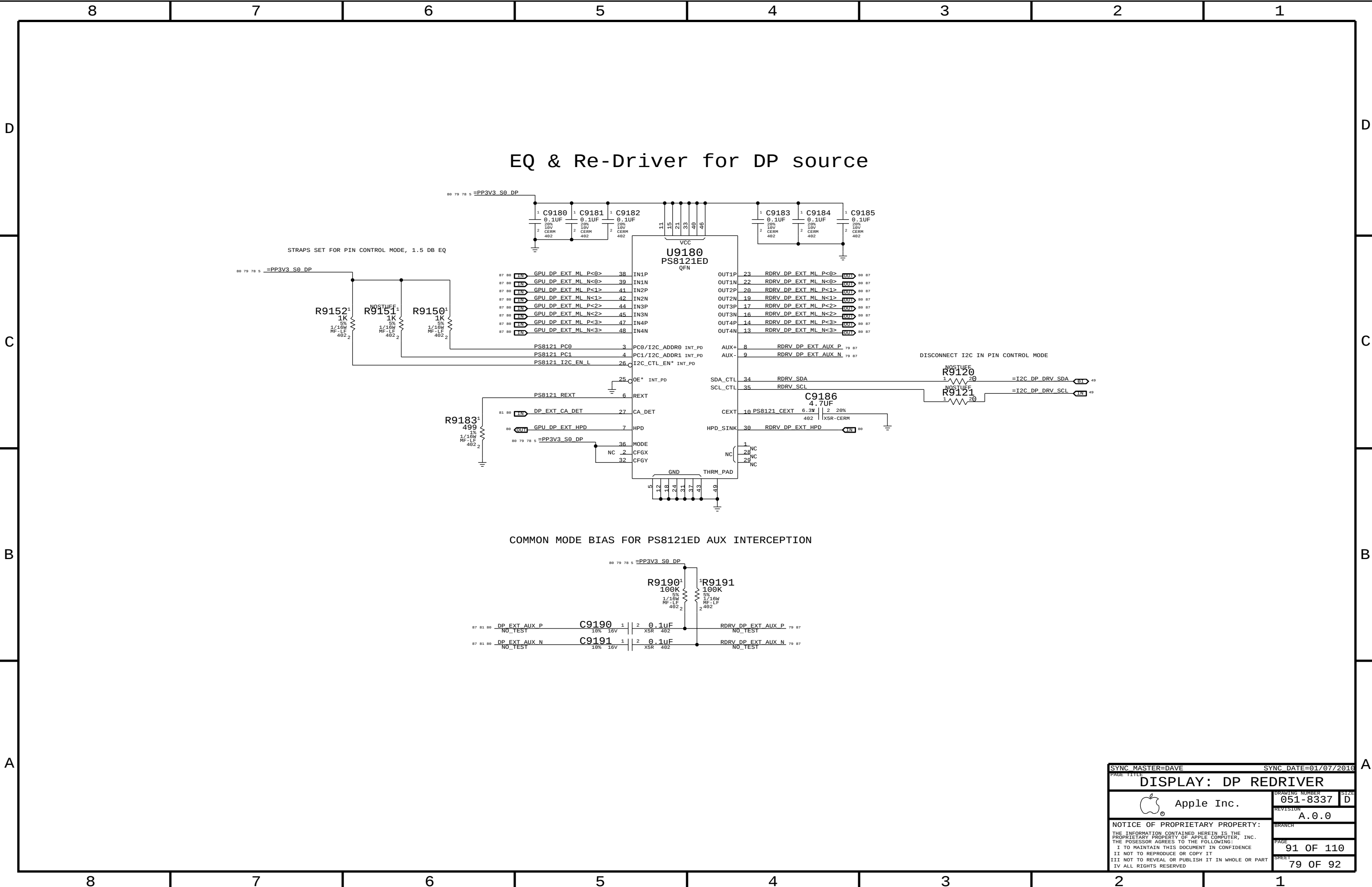
- =SMB_DP_TCON_SCL, =SMB_DP_TCON_SDA

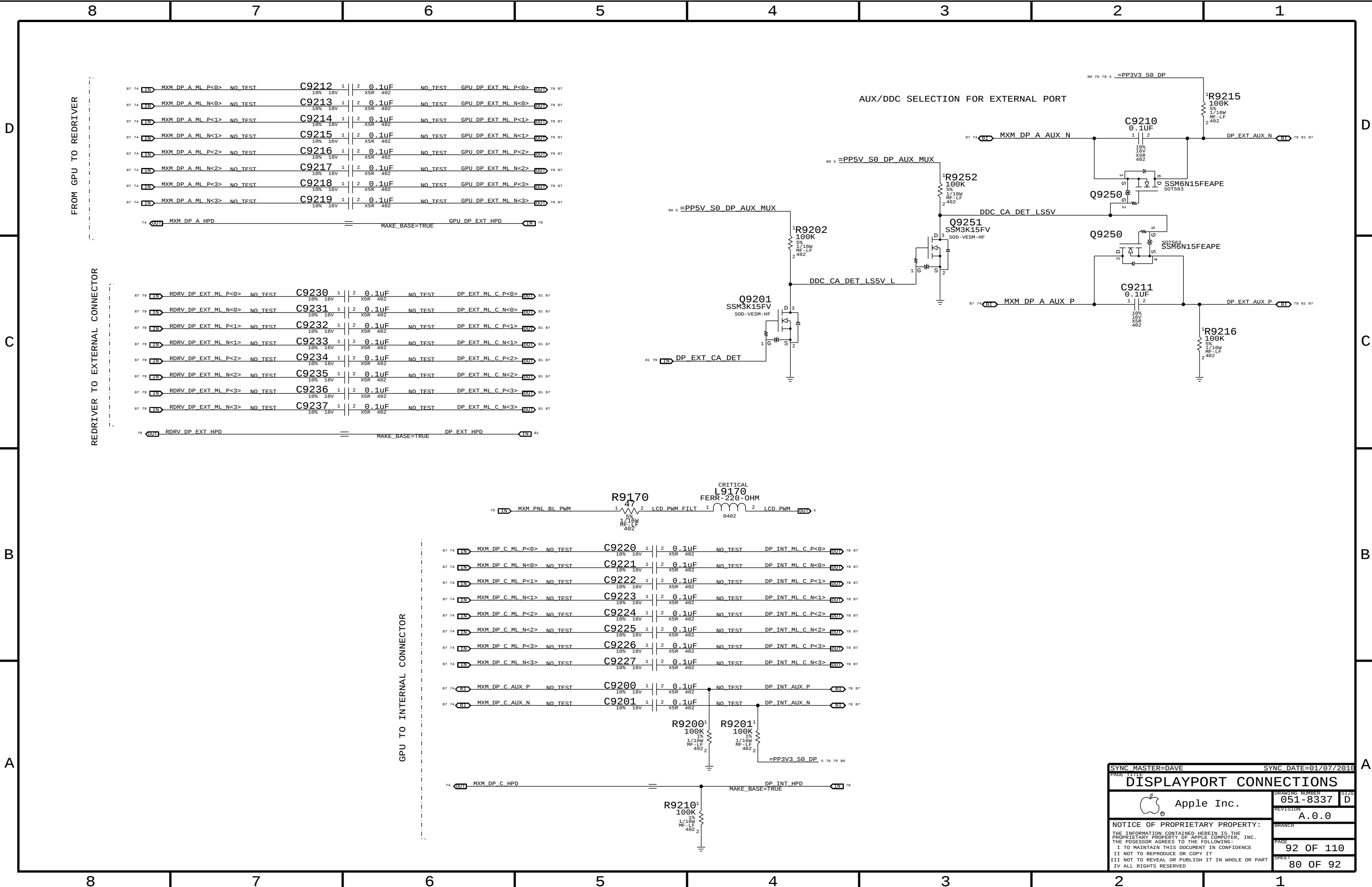
BOM options provided by this page:

guarantee backlight is
only on when Panel has valid video



SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE 171		PAGE 171	
Display: Int DP Connector			
 Apple Inc.		DRAWING NUMBER 051-8337	
		SIZE D	
		REVISION A.0.0	
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SYNC MASTER=DAVE

SYNC DATE=01/07/2016

PAGE TITLE

DISPLAYPORT CONNECTIONS

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DRAWING NUMBER
051-8337

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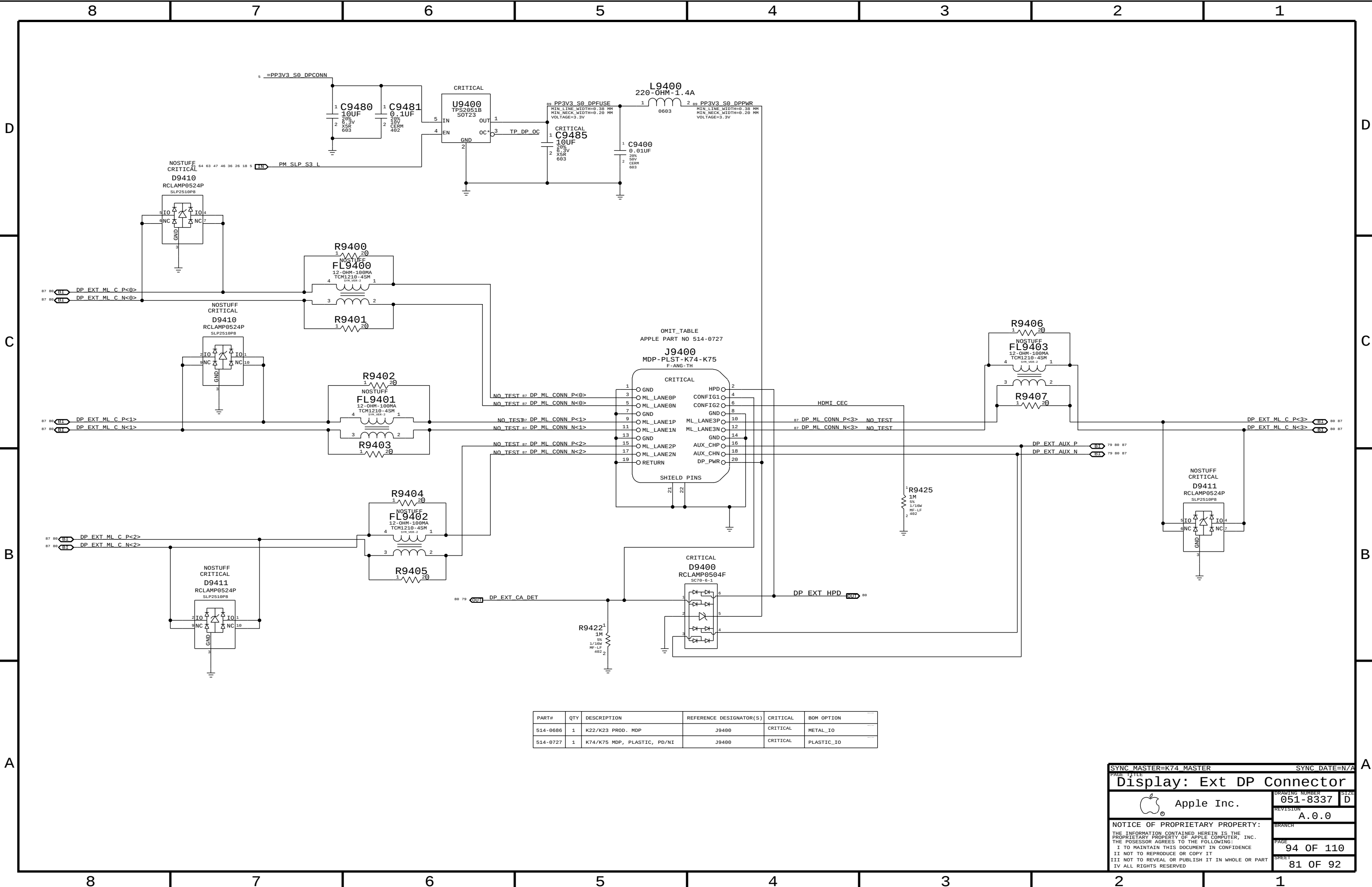
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0686	1	K22/K23 PROD. MDP	J9400	CRITICAL	METAL_IO
514-0727	1	K74/K75 MDP, PLASTIC, PD/NI	J9400	CRITICAL	PLASTIC_IO

SYNC MASTER=K74 MASTER

SYNC DATE=N/A

Display: Ext DP Connector

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051-8337

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_35S	*	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING RULE SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
------------------	-------	----------------------	--------

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DQ_00D2DQ_ODD	*	=3:1_SPACING	?
MEM_DQ_ODD2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_EVEN	*	=3:1_SPACING	?
MEM_DQ_EVEN2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_ODD	*	=5:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20THER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_ODD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_EVEN	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_ODD	MEM_CLK	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CTRL	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CMD	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_ODD	*	MEM_DQ_ODD2DQ_ODD
MEM_DQ_ODD	MEM_DQS	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM	MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL	MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM	MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CTRL	MEM_DQ_ODD	*	MEM_CTRL2MEM	MEM_CMD	MEM_DQ_ODD	*	MEM_CMD2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM	MEM_CMD	MEM_DQS	*	MEM_CMD2MEM
MEM_CTRL	MEM_DQ_EVEN	*	MEM_CTRL2MEM	MEM_CMD	MEM_DQ_EVEN	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20OTHER
MEM_CTRL	*	*	MEM_20OTHER
MEM_CMD	*	*	MEM_20OTHER
MEM_DQ_ODD	*	*	MEM_20OTHER
MEM_DQS	*	*	MEM_20OTHER
MEM_DQ_EVEN	*	*	MEM_20OTHER

Need to support MEM_*-style wildcards!

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER_PHY	*	MEM_POWER_WIDTH	MEM_POWER	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_RCOMP_PHY	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_RCOMP	*	0.2 MM	?

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	MEM 780	MEM CLK	MEM A CLK P<3..0>	11 32
	MEM 780	MEM CLK	MEM A CLK N<3..0>	11 32
	MEM 395	MEM CTRL	MEM A CKE<3..0>	11 30
	MEM 395	MEM CTRL	MEM A CS L<3..0>	11 30
	MEM 395	MEM CTRL	MEM A ODT<3..0>	11 30
	MEM 355	MEM CMD	MEM A A<15..0>	11 30
	MEM 355	MEM CMD	MEM A BA<2..0>	11 30
	MEM 355	MEM CMD	MEM A RAS L	11 30
	MEM 355	MEM CMD	MEM A CAS L	11 30
	MEM 355	MEM CMD	MEM A WE L	11 31
	MEM 455	MEM DQ EVEN	MEM A DQ<7..0>	11 32
	MEM 455	MEM DQ EVEN	MEM A DM<0>	11 32
	MEM 455	MEM DQ_ODD	MEM A DQ<15..8>	11 32
	MEM 455	MEM DQ_ODD	MEM A DM<1>	11 32
	MEM 455	MEM DQ EVEN	MEM A DQ<23..16>	11 32
	MEM 455	MEM DQ EVEN	MEM A DM<2>	11 32
	MEM 455	MEM DQ_ODD	MEM A DQ<31..24>	11 32
	MEM 455	MEM DQ_ODD	MEM A DM<3>	11 32
	MEM 455	MEM DQ EVEN	MEM A DQ<39..32>	11 32
	MEM 455	MEM DQ EVEN	MEM A DM<4>	11 32
	MEM 455	MEM DQ_ODD	MEM A DQ<47..40>	11 32
	MEM 455	MEM DQ_ODD	MEM A DM<5>	11 32
	MEM 455	MEM DQ EVEN	MEM A DQ<55..48>	11 32
	MEM 455	MEM DQ EVEN	MEM A DM<6>	11 32
	MEM 455	MEM DQ_ODD	MEM A DQ<63..56>	11 32
	MEM 455	MEM DQ_ODD	MEM A DM<7>	11 32
	MEM 780	MEM DQS	MEM A DQS P<0>	11 32
	MEM 780	MEM DQS	MEM A DQS N<0>	11 32
	MEM 780	MEM DQS	MEM A DQS P<1>	11 32
	MEM 780	MEM DQS	MEM A DQS N<1>	11 32
	MEM 780	MEM DQS	MEM A DQS P<2>	11 32
	MEM 780	MEM DQS	MEM A DQS N<2>	11 32
	MEM 780	MEM DQS	MEM A DQS P<3>	11 32
	MEM 780	MEM DQS	MEM A DQS N<3>	11 32
	MEM 780	MEM DQS	MEM A DQS P<4>	11 32
	MEM 780	MEM DQS	MEM A DQS N<4>	11 32
	MEM 780	MEM DQS	MEM A DQS P<5>	11 32
	MEM 780	MEM DQS	MEM A DQS N<5>	11 32
	MEM 780	MEM DQS	MEM A DQS P<6>	11 32
	MEM 780	MEM DQS	MEM A DQS N<6>	11 32
	MEM 780	MEM DQS	MEM A DQS P<7>	11 32
	MEM 780	MEM DQS	MEM A DQS N<7>	11 32
	MEM 780	MEM CLK	MEM B CLK P<3..0>	11 32
	MEM 780	MEM CLK	MEM B CLK N<3..0>	11 32
	MEM 395	MEM CTRL	MEM B CKE<3..0>	11 31
	MEM 395	MEM CTRL	MEM B CS L<3..0>	11 31
	MEM 395	MEM CTRL	MEM B ODT<3..0>	11 31
	MEM 355	MEM CMD	MEM B A<15..0>	11 31
	MEM 355	MEM CMD	MEM B BA<2..0>	11 31
	MEM 355	MEM CMD	MEM B RAS L	11 31
	MEM 355	MEM CMD	MEM B CAS L	11 31
	MEM 355	MEM CMD	MEM B WE L	11 31
	MEM 455	MEM DQ EVEN	MEM B DQ<7..0>	11 32
	MEM 455	MEM DQ EVEN	MEM B DM<0>	11 32
	MEM 455	MEM DQ_ODD	MEM B DQ<15..8>	11 32
	MEM 455	MEM DQ_ODD	MEM B DM<1>	11 32
	MEM 455	MEM DQ EVEN	MEM B DQ<23..16>	11 32
	MEM 455	MEM DQ EVEN	MEM B DM<2>	11 32
	MEM 455	MEM DQ_ODD	MEM B DQ<31..24>	11 32
	MEM 455	MEM DQ_ODD	MEM B DM<3>	11 32
	MEM 455	MEM DQ EVEN	MEM B DQ<39..32>	11 32
	MEM 455	MEM DQ EVEN	MEM B DM<4>	11 32
	MEM 455	MEM DQ_ODD	MEM B DQ<47..40>	11 32
	MEM 455	MEM DQ_ODD	MEM B DM<5>	11 32
	MEM 455	MEM DQ EVEN	MEM B DQ<55..48>	11 32
	MEM 455	MEM DQ EVEN	MEM B DM<6>	11 32
	MEM 455	MEM DQ_ODD	MEM B DQ<63..56>	11 32
	MEM 455	MEM DQ_ODD	MEM B DM<7>	11 32

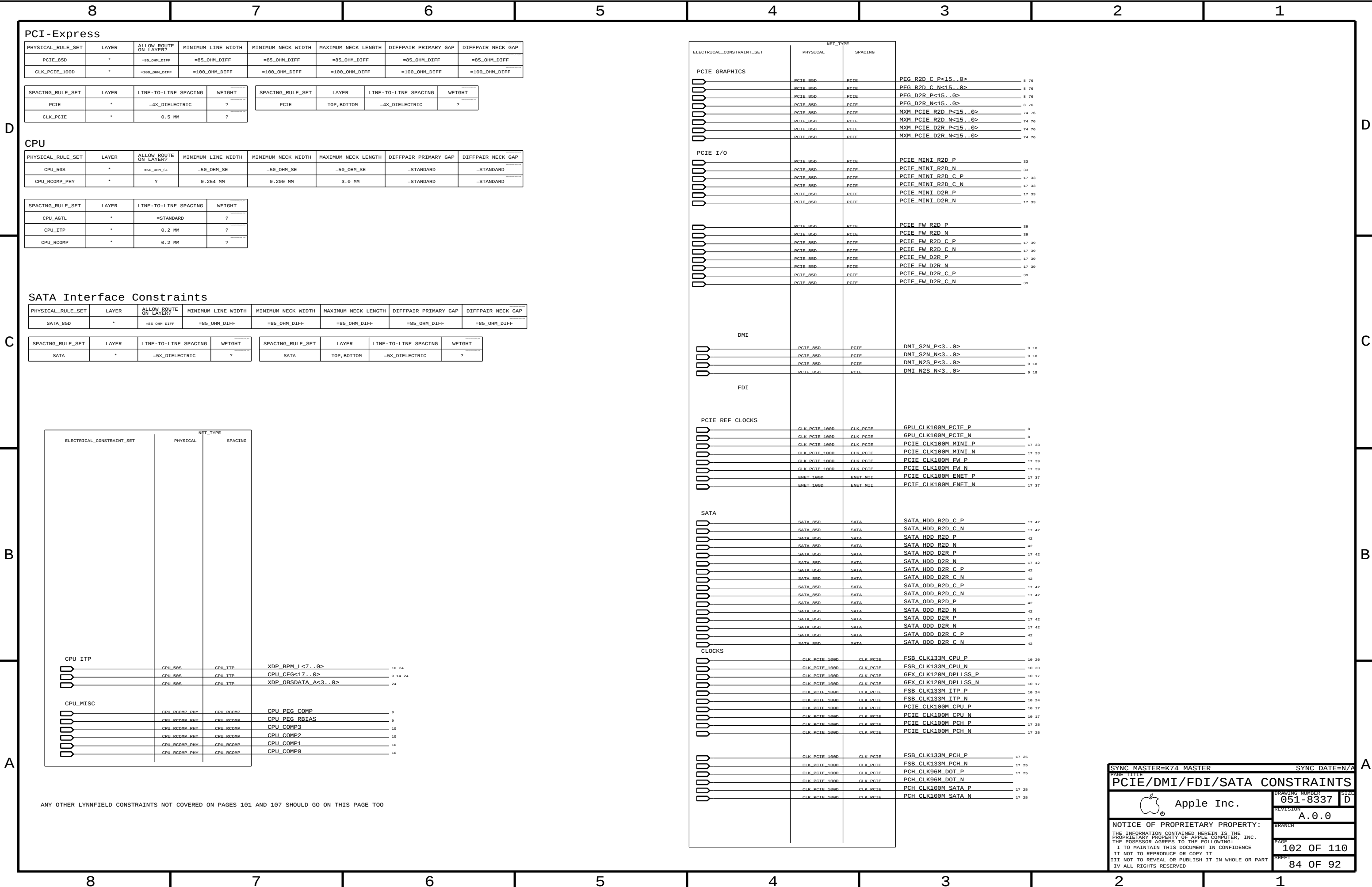
MEMORY POWER PROPERTIES

NET_TYPE			
VOLTAGE	PHYSICAL	SPACING	
	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A 11 28
	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B 11 28

Memory Net Properties

		NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	MEM_780	MEM_DQS	MEM_B_DQS_P<0>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_N<0>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_P<1>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_N<1>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_P<2>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_N<2>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_P<3>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_N<3>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_P<4>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_N<4>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_P<5>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_N<5>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_P<6>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_N<6>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_P<7>	11 32
	MEM_780	MEM_DQS	MEM_B_DQS_N<7>	11 32
R150	MEM_RCAMP_PHY	MEM_RCAMP	CPU_SM_RCAMP0	10
R159	MEM_RCAMP_PHY	MEM_RCAMP	CPU_SM_RCAMP1	10
R163	MEM_RCAMP_PHY	MEM_RCAMP	CPU_SM_RCAMP2	10

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
Memory Constraints			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-8337	D
		REVISION	
		A.0.0	
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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	0.2 MM	?
COMP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

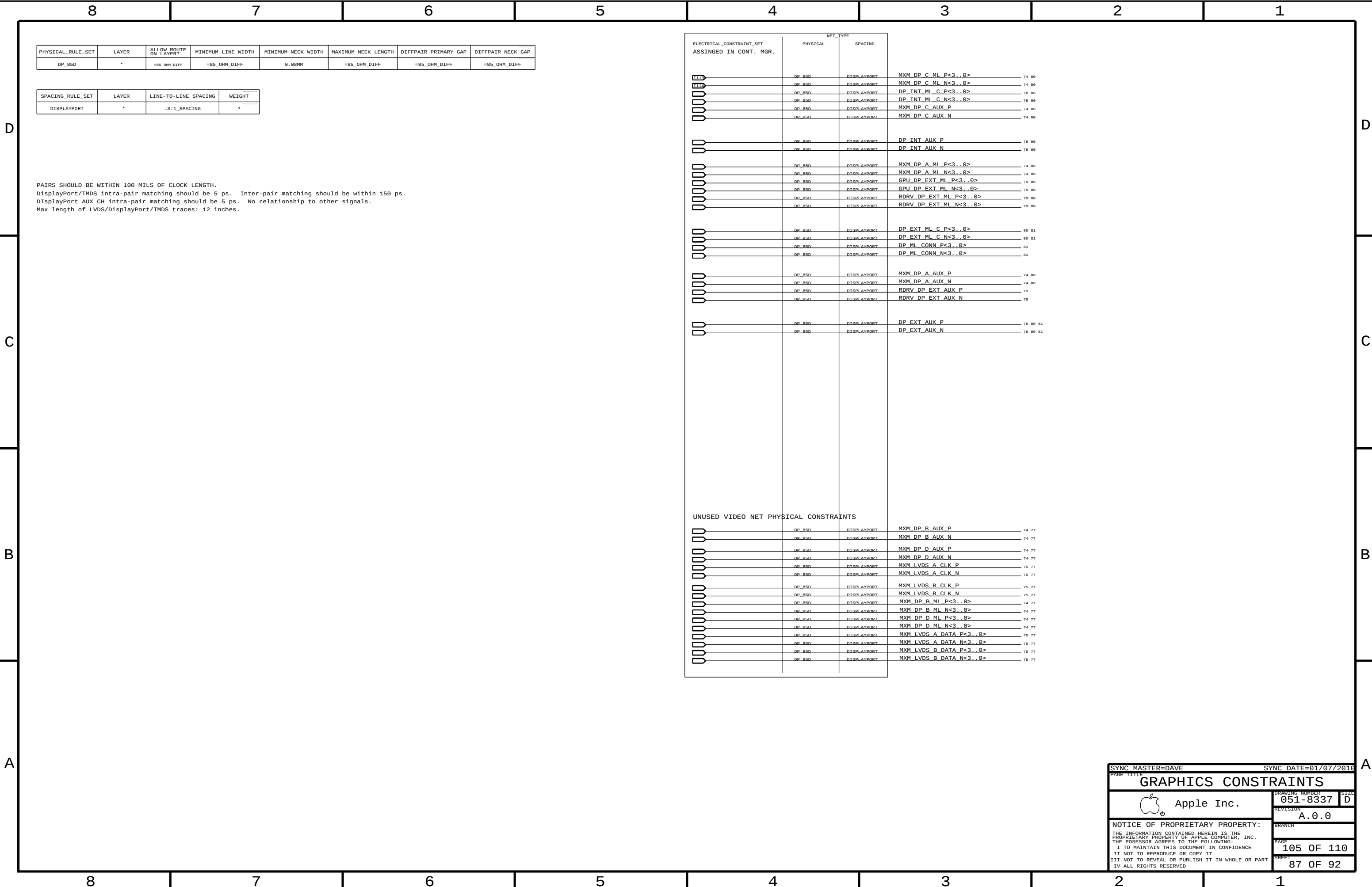
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE SPACING		
	PCI_55S	PCI	PCI REQ0_L	19
	PCI_55S	PCI	PCI REQ1_L	19
	CLK_PCI_55S	CLK_PCI	PCH CLK33M PCIOUT	19 27
	CLK_PCI_55S	CLK_PCI	PCH CLK33M PCIIIN	19 27
	LPC_55S	LPC	LPC AD<3..0>	17 46 48
	LPC_55S	LPC	LPC FRAME_L	17 46 48
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC_R	19 27
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	27 46
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	27 48
	CLK_LPC_55S	PM	PM CLK32K SUSCLK_R	8 18 91
	CLK_LPC_55S	PM	PM CLK32K SUSCLK	8 46 91
	CLK_LPC_55S	CLK_LPC	LPCLCK33M LPCPLUS_R	19 27
	USB_900	USB	USB EXTA_P	34 43
	USB_900	USB	USB EXTA_N	34 43
	USB_900	USB	USB PORT0_P	43
	USB_900	USB	USB PORT0_N	43
	USB_900	USB	USB EXTB_P	35 43
	USB_900	USB	USB EXTB_N	35 43
	USB_900	USB	USB PORT1_P	43
	USB_900	USB	USB PORT1_N	43
	USB_900	USB	USB EXTC_P	34 43
	USB_900	USB	USB EXTC_N	34 43
	USB_900	USB	USB PORT2_P	43
	USB_900	USB	USB PORT2_N	43
	USB_900	USB	USB EXTD_P	35 43
	USB_900	USB	USB EXTD_N	35 43
	USB_900	USB	USB D_MUXED_P	43
	USB_900	USB	USB D_MUXED_N	43
	USB_900	USB	USB PORT3_P	43
	USB_900	USB	USB PORT3_N	43
	USB_900	USB	USB CAMERA_P	34 44
	USB_900	USB	USB CAMERA_N	34 44
	USB_900	USB	USB CAMERA_L_P	44 92
	USB_900	USB	USB CAMERA_L_N	44 92
	USB_900	USB	USB BT_P	35 44
	USB_900	USB	USB BT_N	35 44
	USB_900	USB	USB_BT_L_P	44 92
	USB_900	USB	USB_BT_L_N	44 92
	USB_900	USB	USB_IR_P	34 44
	USB_900	USB	USB_IR_N	34 44
	USB_900	USB	USB_IR_L_P	44 92
	USB_900	USB	USB_IR_L_N	44 92
	USB_900	USB	USB_SDCARD_P	35 44
	USB_900	USB	USB_SDCARD_N	35 44
	USB_900	USB	USB_SDCARD_L_P	44 92
	USB_900	USB	USB_SDCARD_L_N	44 92
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	17 27
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	17 27
	CLK_XTAL	XTAL	CK505_XTAL_IN	25
	CLK_XTAL	XTAL	CK505_XTAL_OUT	25
	CLK_PCH_55S	CLK_PCH	PCH_CLK14P3M_REFCLK	17 25
	USB_900	USB	USB_HUB1_UP_P	19 34
	USB_900	USB	USB_HUB1_UP_N	19 34
	USB_900	USB	USB_HUB2_UP_P	19 35
	USB_900	USB	USB_HUB2_UP_N	19 35

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CB

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

		ET_TYPE		
	PHYSICAL	SPACING	VOLTAGE	
HEB0	POWER	SWITCHNODE	1.5V	VR CPU PHASE1
HEB0	POWER	SWITCHNODE	1.5V	VR CPU PHASE2
HEB0	POWER	SWITCHNODE	1.5V	VR CPU PHASE3
HEB0	POWER	SWITCHNODE	3.3V	P3V3S5 REG PHASE
HEB0	POWER	SWITCHNODE	5V	P5V3S3 REG PHASE
HEB0	POWER	SWITCHNODE	1.1V	VTT REG PHASE
HEB0	POWER	SWITCHNODE	3.4V	P3V42G3H SW
HEB0	POWER	SWITCHNODE	1.05V	PCHCORE REG PHASE
HEB0	POWER	SWITCHNODE	1.5V	DDR REG PHASE
HEB0	POWER	SWITCHNODE	1.8V	P1V8 REG PHASE
HEB0	POWER	POWER	1.5V	PP0V75 S3 MEM VREFCA A
HEB0	POWER	POWER	1.5V	PP0V75 S3 MEM VREFCA B
HEB0	POWER	POWER	1.5V	PP0V75 S3 MEM VREFD0 A
HEB0	POWER	POWER	1.5V	PP0V75 S3 MEM VREFD0 B
HEB0	POWER	POWER	12V	PP12V AUD SPKRAMP PLANE
HEB0	POWER	POWER	12V	PP12V S0
HEB0	POWER	POWER	12V	PP12V S0 CPU FLTRD
HEB0	POWER	POWER	12V	PP12V S0 FAN0 L
HEB0	POWER	POWER	12V	PP12V S0 FAN1 L
HEB0	POWER	POWER	12V	PP12V S0 FAN2 L
HEB0	POWER	POWER	12V	PP12V G3H
HEB0	POWER	POWER	12V	PP12V S5
HEB0	POWER	POWER	12V	FW PORT0 VP
HEB0	POWER	POWER	12V	FW PORT0 VP F
HEB0	POWER	POWER	12V	PPVP FW PHY CPS
HEB0	POWER	POWER	1.1V	PVPCORE S0 CPU REG1
HEB0	POWER	POWER	1.1V	PVPCORE S0 CPU REG2
HEB0	POWER	POWER	1.1V	PVPCORE S0 CPU REG3
HEB0	POWER	POWER	1.05V	PP1V05 S0
HEB0	POWER	POWER	1.05V	PP1V05 S0 CK505 F
HEB0	POWER	POWER	1.05V	PP1V05 S0 PCH VCCADPLL A
HEB0	POWER	POWER	1.05V	PP1V05 S0 PCH VCCADPLL B
HEB0	POWER	POWER	1.05V	PP1V05 S0 PCH VCCAPLL EXP
HEB0	POWER	POWER	1.05V	PP1V05 S0 PCH VCCAPLL FDI
HEB0	POWER	POWER	1.05V	PP1V05 S0 PCH VCCAPLL SATA
HEB0	POWER	POWER	1.05V	PP1V05 S0 PCH VCCA CLK
HEB0	POWER	POWER	1.05V	PP1V05 SM PCH LAN
HEB0	POWER	POWER	1.1V	PPVTT S0
HEB0	POWER	POWER	0.75V	PPVTT S0 DDR
HEB0	POWER	POWER	0.75V	PP0V75 S0
HEB0	POWER	POWER	1.5V	PP1V5 S0
HEB0	POWER	POWER	1.5V	PP1V5 S0 CK505 F
HEB0	POWER	POWER	1.5V	PP1V5 S0 CK505 R
HEB0	POWER	POWER	1.5V	PP1V5 S3
HEB0	POWER	POWER	1.5V	PP1V5 CPU MEM
HEB0	POWER	POWER	1.5V	PP1V8R1V5 S0 PCH VCCVRM
HEB0	POWER	POWER	1.5V	PP1V5 FW VDDA
HEB0	POWER	POWER	1.5V	PP1V8 S0
HEB0	POWER	POWER	1.96V	PP1V96 FW PLLVDD
HEB0	POWER	POWER	1.96V	PP1V95 FW FWPHY

POWER NET PROPERTIES

NET_TYPE			
PHYSICAL	SPACING	VOLTAGE	
PP3V3	POWER	3.3V	PP3V3_S0
PP3V3	POWER	3.3V	PP3V3_S0_CK505_F
PP3V3	POWER	3.3V	PP3V3_S0_DPFSUSE
PP3V3	POWER	3.3V	PP3V3_S0_DPPWR
PP3V3	POWER	3.3V	PP3V3_S0_HS_F
PP3V3	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC
PP3V3	POWER	3.3V	PP3V3_S0_TSENS_R
PP3V3	POWER	3.3V	PP3V3_S3
PP3V3	POWER	3.3V	PP3V3_S3_BT_FLT
PP3V3	POWER	3.3V	PP3V3_S3_SDCARD_FLT
PP3V3	POWER	3.3V	PP3V3_S5
PPVTT	POWER	3.3V	PPVTT_S3_DDR_BUF
PPV	POWER	3.3V	PPV_S0_MXM_PWRSRC
PPVOUT	POWER	3.3V	PPVOUT_S0_PCH_DCPSSRT
PPVOUT	POWER	3.3V	PPVOUT_S5_PCH_DCPSSRT
PPVOUT	POWER	3.3V	PPVOUT_S5_PCH_DCPSSUSBYP
PPVOUT	POWER	3.3V	PPVOUT_G3_PCH_DCPRTIC
PPVOUT	POWER	3.3V	PPVOUT_S0_PCH_VCCRTC_NTC
PPVBATT	POWER	3.3V	PPVBATT_G3_RTC
PPVBATT	POWER	3.3V	PPVBATT_G3_RTC_R
PP3V3	POWER	3.3V	PP3V3_AUDIO_SPDIF_JACK
PP3V3	POWER	3.3V	PP3V3_FW_AVDD
PP3V3	POWER	3.3V	PP3V3_FW_ESD
PP3V3	POWER	3.3V	PP3V3_FW_PLLVDD
PP3V3	POWER	3.3V	PP3V3_FW_VDDA
PP3V3	POWER	3.3V	PP3V3_G3_RTC
PP	POWER	3.3V	PP_ENET_CTRL12
PP3V3	POWER	3.4V	PP3V3_G3H_SMC_AVCC
PP3V3	POWER	3.3V	PP3V3_G3H_AVREF_SMC
PP3V42	POWER	3.42V	PP3V42_G3H
4V5	POWER	4.5V	4V5_REG_IN
PP4V5	POWER	4.5V	PP4V5_AUDIO_ANALOG
PP5V	POWER	5V	PP5V_S0
PP5V	POWER	5V	PP5V_S0_CPU_VCORE_VCC
PP5V	POWER	5V	PP5V_S0_PCH_V5REF
PP5V	POWER	5V	PP5V_S3
PP5V	POWER	5V	PP5V_S3_DDR_REG_V5FLT
PP5V	POWER	5V	PP5V_S3_CAMERA_FLT
PP5V	POWER	5V	PP5V_S3_IR_FLT
PP5V	POWER	5V	PP5V_S5
PP5V	POWER	5V	PP5V_S5_PCH_V5REFSUS
PP5V	POWER	5V	PP5V_USB2_PORT0
PP5V	POWER	5V	PP5V_USB2_PORT0_F
PP5V	POWER	5V	PP5V_USB2_PORT1
PP5V	POWER	5V	PP5V_USB2_PORT1_F
PP5V	POWER	5V	PP5V_USB2_PORT2
PP5V	POWER	5V	PP5V_USB2_PORT2_F
PP5V	POWER	5V	PP5V_USB2_PORT3
PP5V	POWER	5V	PP5V_USB2_PORT3_F
DDR_REG	POWER		DDR_REG_PGND
DDR_REG	POWER		DDR_REG_CSGND

SENSING NET PROPERTIES

NET_TYPE		PHYSICAL	SPACING		
IE63D	SNS_DIFF	THERMAL	VR CPU ISNS1 P	05	06
IE63D	SNS_DIFF	THERMAL	VR CPU ISNS1 N	05	06
IE63D	SNS_DIFF	THERMAL	VR CPU ISNS1 R P	05	
IE63D	SNS_DIFF	THERMAL	VR CPU ISNS1 R N	05	
IE63D	SNS_DIFF	THERMAL	VR CPU ISNS2 P	05	06
IE63D	SNS_DIFF	THERMAL	VR CPU ISNS2 N	05	06
IE63D	SNS_DIFF	THERMAL	VR CPU ISNS2 R P	05	
IE63D	SNS_DIFF	THERMAL	VR CPU ISNS2 R N	05	
IE63D	SNS_DIFF	THERMAL	VR CPU ISNS3 P	05	06
IE63D	SNS_DIFF	THERMAL	VR CPU ISNS3 N	05	06
IE63D	SNS_DIFF	THERMAL	VR CPU ISNS3 R P	05	
IE63D	SNS_DIFF	THERMAL	VR CPU ISNS3 R N	05	
IE63D	SNS_DIFF				
IE63D	SNS_DIFF		VR CPU VSEN	05	
IE63D	SNS_DIFF		VR CPU RGND	05	
IE63D	SNS_DIFF		VR CPU VSNS R N	05	
IE63D	SNS_DIFF		VR CPU VSNS R P	05	
IE63D	SNS_DIFF		VR CPU VSNS XW P	05	
IE63D	SNS_DIFF		VR CPU VSNS XW N	05	
IE63D	SNS_DIFF				
IE63D	SNS_DIFF		CPU VCC_PKG_SENSE P	12	05 06
IE63D	SNS_DIFF		CPU VCC_PKG_SENSE N	12	05 06
IE63D	SNS_DIFF		VTT REG ISNS P		
IE63D	SNS_DIFF		VTT REG ISNS N		
IE63D	SNS_DIFF		CPU VTTSENSE P	12	08
IE63D	SNS_DIFF		CPU VTTSENSE N	12	08
IE63D	SNS_DIFF		CPU VTTSENSE R P		
IE63D	SNS_DIFF		CPU VTTSENSE R N		
IE63D	SNS_DIFF		VTT REG VSEN		
IE63D	SNS_DIFF		VTT REG RGND		
IE63D	SNS_DIFF		VTT REG RT01		
IE63D	SNS_DIFF		VTT REG RTR1		

VR CTRL NET PROPERTIES

		NET_TYPE	
PHYSICAL		SPACING	
	VR_CTL_PHY	VR_CTL	VR CPU PH1 SNUB
E622	VR_CTL_PHY	VR_CTL	VR CPU PH2 SNUB
E623	VR_CTL_PHY	VR_CTL	VR CPU PH3 SNUB
	VR_CTL_PHY	VR_CTL	VR CPU PWM1
E624	VR_CTL_PHY	VR_CTL	VR CPU PWM2
E625	VR_CTL_PHY	VR_CTL	VR CPU PWM2_R
E626	VR_CTL_PHY	VR_CTL	VR CPU PWM3
E627	VR_CTL_PHY	VR_CTL	VR CPU PWM3_R
	VR_CTL_PHY	VR_CTL	VR CPU PWM4_R
E628	VR_CTL_PHY	VR_CTL	VR CPU REF
E629	VR_CTL_PHY	VR_CTL	VR CPU SS
E630	VR_CTL_PHY	VR_CTL	VR CPU TCOMP
E631	VR_CTL_PHY	VR_CTL	VR CPU TM
E632	VR_CTL_PHY	VR_CTL	VR CPU BOOT1_RC
E633	VR_CTL_PHY	VR_CTL	VR CPU BOOT2_RC
E634	VR_CTL_PHY	VR_CTL	VR CPU BOOT3_RC
E635	VR_CTL_PHY	VR_CTL	VR CPU COMP
E636	VR_CTL_PHY	VR_CTL	VR CPU COMP_R
	VR_CTL_PHY	VR_CTL	VR CPU COMP_RC
E637	VR_CTL_PHY	VR_CTL	VR CPU DAC
E638	VR_CTL_PHY	VR_CTL	VR CPU DRV1_BOOT
E639	VR_CTL_PHY	VR_CTL	VR CPU DRV1_GDSEL
E640	VR_CTL_PHY	SWITCHNODE	VR CPU DRV1_LGATE
	VR_CTL_PHY	SWITCHNODE	VR CPU DRV1_UGATE
E641	VR_CTL_PHY	VR_CTL	VR CPU DRV2_BOOT
	VR_CTL_PHY		VR CPU DRV2_GDSEL
E642	VR_CTL_PHY	SWITCHNODE	VR CPU DRV2_LGATE
	VR_CTL_PHY	SWITCHNODE	VR CPU DRV2_UGATE
	VR_CTL_PHY	VR_CTL	VR CPU DRV3_BOOT
E643	VR_CTL_PHY	VR_CTL	VR CPU DRV3_GDSEL
E644	VR_CTL_PHY	SWITCHNODE	VR CPU DRV3_LGATE
	VR_CTL_PHY	SWITCHNODE	VR CPU DRV3_UGATE
	VR_CTL_PHY	VR_CTL	VR CPU FAN
E645	VR_CTL_PHY	VR_CTL	VR CPU FB
E646	VR_CTL_PHY	VR_CTL	VR CPU FB_R
E647	VR_CTL_PHY	VR_CTL	VR CPU FS
E648	VR_CTL_PHY	VR_CTL	VR CPU IMON
	VR_CTL_PHY	VR_CTL	VR CPU TOUT_PD
E649	VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_UGATE
E650	VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_LGATE
E651	VR_CTL_PHY	VR_CTL	PCHCORE_REG_VFB
	VR_CTL_PHY	VR_CTL	PCHCORE_REG_TON
E652	VR_CTL_PHY	VR_CTL	PCHCORE_REG_TRIP
E653	VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT_R
	VR_CTL_PHY	VR_CTL	VTT REG BOOT
E654	VR_CTL_PHY	VR_CTL	VTT REG COMP
E655	VR_CTL_PHY	VR_CTL	VTT REG FB
E656	VR_CTL_PHY	VR_CTL	VTT REG FS
E657	VR_CTL_PHY	VR_CTL	VTT REG COMP
E658	VR_CTL_PHY	VR_CTL	VTT REG REF
	VR_CTL_PHY	SWITCHNODE	VTT REG LGATE
E659	VR_CTL_PHY	VR_CTL	VTT REG_OCSET
E660	VR_CTL_PHY	VR_CTL	VTT_OFS
E661	VR_CTL_PHY	VR_CTL	VTT_REF_REF
	VR_CTL_PHY	VR_CTL	VTT_REF_UGATE
E662	VR_CTL_PHY	VR_CTL	VTT_REF_PH1_SNUB
	VR_CTL_PHY	VR_CTL	P3V42G3H_BOOST
E663	VR_CTL_PHY	VR_CTL	P3V42G3H_FB

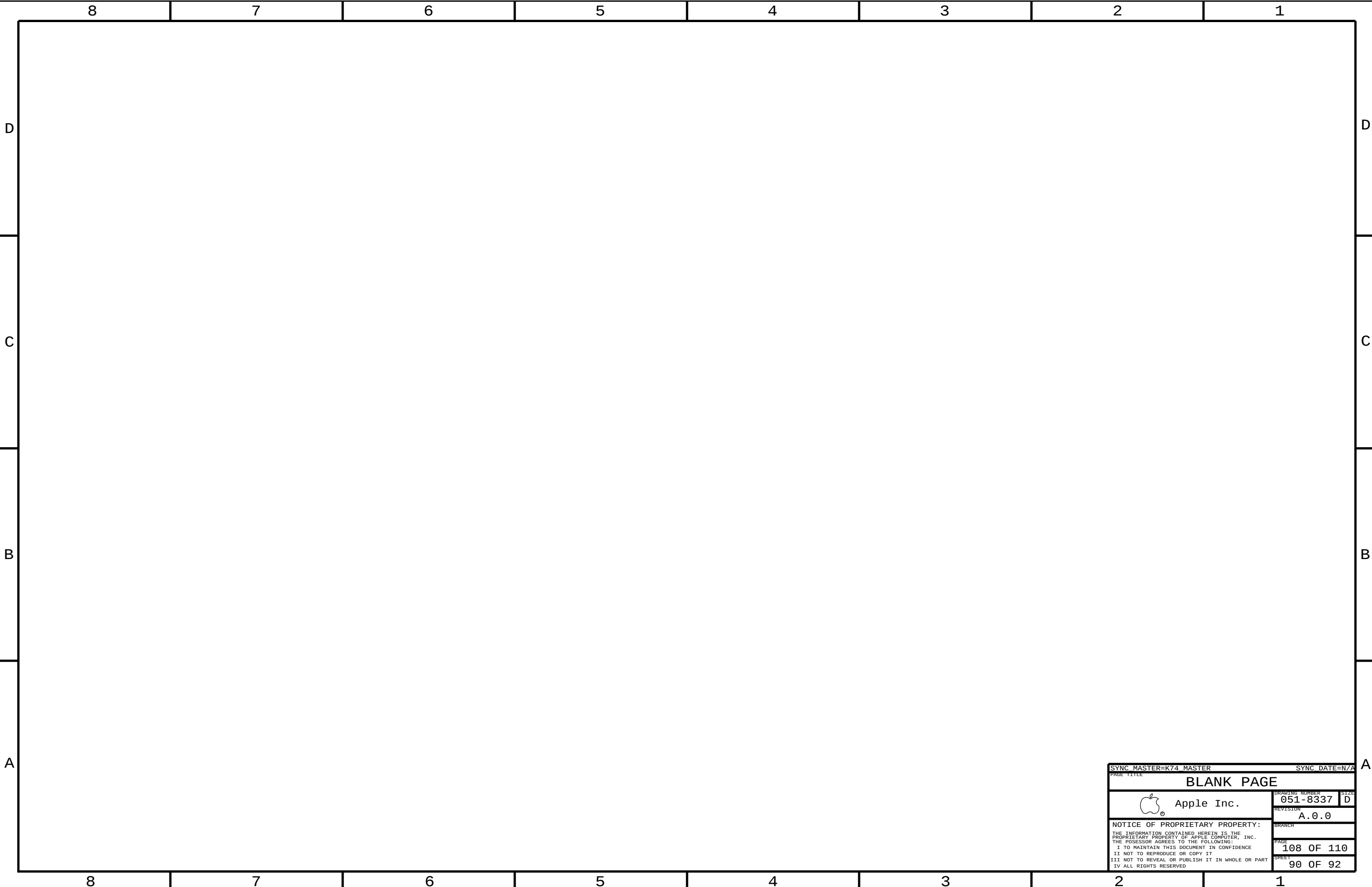
VR CTRL NET PROPERTIES

NET_TYPE				
PHYSICAL		SPACING		
REG0	VR_CTL_PHY	VR_CTL	DDR REG CS	71
REG0	VR_CTL_PHY	VR_CTL	DDR REG FB	71
REG0	VR_CTL_PHY	SWITCHNODE	DDR REG LGATE	71
REG0	VR_CTL_PHY	SWITCHNODE	DDR REG UGATE	71
REG0	VR_CTL_PHY	VR_CTL	DDR REG BOOT	71
REG0	VR_CTL_PHY	VR_CTL	DDR REG BOOT R	71
REG0	VR_CTL_PHY	VR_CTL	DDR REG VDDOSNS	71
REG0	VR_CTL_PHY	VR_CTL	DDR REG VITSNS	71
REG0	VR_CTL_PHY			
REG0	VR_CTL_PHY	VR_CTL	P1V8 REG POR	71
REG0	VR_CTL_PHY	VR_CTL		
REG0	VR_CTL_PHY	VR_CTL	P3V3S5 REG BOOT	70
REG0	VR_CTL_PHY	VR_CTL	P3V3S5 REG BOOT R	70
REG0	VR_CTL_PHY	VR_CTL	P3V3S5 REG FB	70
REG0	VR_CTL_PHY	VR_CTL	P3V3S5 REG ISEN	70
REG0	VR_CTL_PHY	SWITCHNODE	P3V3S5 REG LGATE	70
REG0	VR_CTL_PHY	VR_CTL	P3V3S5 REG OCSET	70
REG0	VR_CTL_PHY	SWITCHNODE	P3V3S5 REG UGATE	70
REG0	VR_CTL_PHY	VR_CTL	P3V3S5 REG SNUB	70
REG0	VR_CTL_PHY	VR_CTL	P5V3S3 REG BOOT	70
REG0	VR_CTL_PHY	VR_CTL	P5V3S3 REG FB	70
REG0	VR_CTL_PHY	VR_CTL	P5V3S3 REG ISEN	70
REG0	VR_CTL_PHY	SWITCHNODE	P5V3S3 REG LGATE	70
REG0	VR_CTL_PHY	VR_CTL	P5V3S3 REG OCSET	70
REG0	VR_CTL_PHY	SWITCHNODE	P5V3S3 REG UGATE	70
REG0	VR_CTL_PHY			

VR VID NET PROPERTIES

NET_TYPE		PULL-UP STUB < 1-INCH VID LENGTH SKEW < 1-INCH VID LENGTH RANGE< 1 TO 15-INCH	
PHYSICAL	SPACING		
1500	VID_PHY	VR_CTL	CPU VID<0>
1500	VID_PHY	VR_CTL	CPU VID<1>
1500	VID_PHY	VR_CTL	CPU VID<2>
1500	VID_PHY	VR_CTL	CPU VID<3>
1500	VID_PHY	VR_CTL	CPU VID<4>
1500	VID_PHY	VR_CTL	CPU VID<5>
1500	VID_PHY	VR_CTL	CPU VID<6>
1500	VID_PHY	VR_CTL	CPU VID<7>
1500	VID_PHY	VR_CTL	CPU PSI L

SYNC MASTER=K74 MASTER		SYNC DATE=N/A	
PAGE TITLE			
POWER CONSTRAINTS			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8337		D
REVISION		A.0.0	
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		107 OF 110	
		SHEET	
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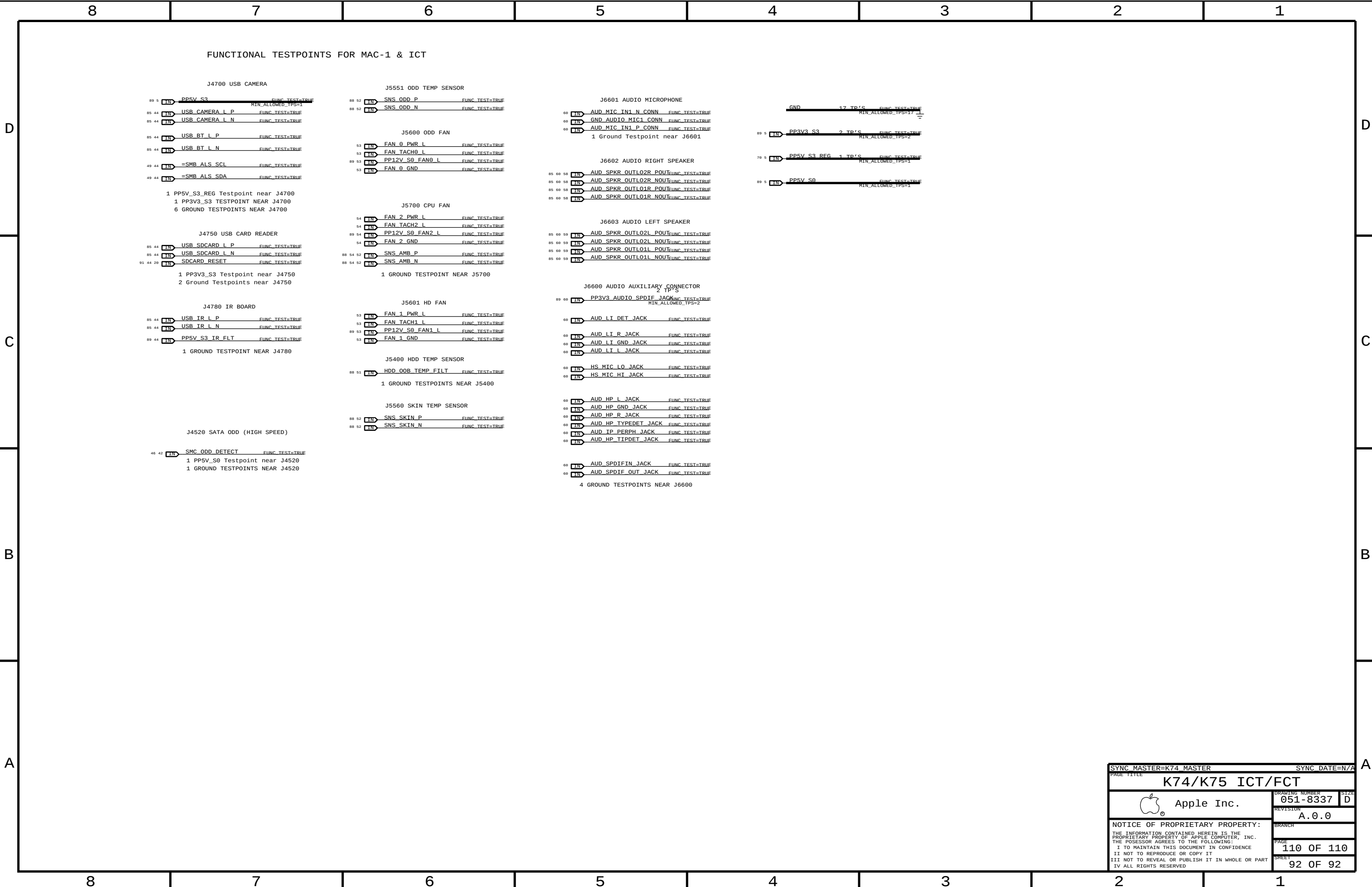
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		REVISION	A.0.0
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		PAGE	108 OF 110
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PM NET PROPERTIES
(PM, RESET, EN, PG00D)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

NET_TYPE			
PHYSICAL	SPACING		
1P	PM	PLT RESET L	19 27
1A	PM_VTT	PLT RESET LS1V1 L	10
1A	PM	PM ADCDC PS_ON	5
1A	PM	PM BATLOW L	14 18 46
1A	PM	PM CLK32K SUSCLK	8 46 85
1A	PM	PM CLK32K SUSCLK_R	8 18 85
1A	PM	PM CLKRUN L	14 18 46 48
1A	PM	PM_EXT TS L<0>	
1A	PM	PM_EXT TS L<1>	
1A	PM	PM_LAN_PWRGD	14 18
1A	PM_VTT	FSB_CPURSTOUT L	10 24
1A	PM_VTT	PM_MEM_PWRGD	10 18
1A	PM	PM_ME_PWRGD	18 64
1A	PM	PM_MXM_PG00D	64 75
1A	PM	PM_PCH_PWRGD	18 64
1A	PM	PM_PG00D_DDRREG_S3	63 71
1A	PM	PM_PG00D_PVCORE_CPU	25 64 65
1A	PM	PM_PWRBTN L	18 24 46
1A	PM	PM_RSMRST L	46 63
1A	PM	PM_RSMRST_PCH L	18 63
1A	PM	PM_SLP_M L	18 63
1A	PM	PM_SLP_S3 L	5 18 26 36 46 47 63 64 81
1A	PM	PM_SLP_S4_1 L	18 63
1A	PM	PM_SLP_S4 L	18 47
1A	PM	PM_SLP_S5 L	18 47
1A	PM	PM_SUS_PWR_ACK	18
1A	PM_VTT	PM_SYNC	10 18
1A	PM	SDCARD_PLT_RST L	27 44
1A	PM	PM_SYSRST L	18 27 46
1A	PM	PM_SYS_PWRGD	18 64
1A	PM_VTT	PM_THRMTRIP L	10 20 47
1A	PM	RSMRST_PWRGD	46 64
1A	PM	RTC RESET L	17 91
1A	PM_VTT	CPU_PWRGD	10 20 24
1A	PM	CPU RESET L	10 27
1A	PM	PG00D_1V8_S0_G1	64
1A	PM	PG00D_1V8_S0_G2	64
1A	PM	PG00D_CPU_GFX_DDR	64
1A	PM	PG00D_P1V5_S0	10 73
1A	PM	PG00D_P1V8_S0	64
1A	PM	PG00D_P3V3_S0	64 73
1A	PM	PG00D_P3V3_S3	34 73
1A	PM	PG00D_P5V_S0	63 73
1A	PM	PG00D_PCH_AND_P1V8	64
1A	PM	PG00D_PCH_S0	64
1A	PM	PG00D_SYSPWROK	64
1A	PM	PG00D_SYSPWROK_R	64
1A	PM	RTC RESET L	17 91
1A	PM	P12V_S3_EN	
1A	PM	P1V5_S0_EN	63 73
1A	PM	P3V3S0_EN	63 73
1A	PM	P3V3S3_EN	63 73
1A	PM	P5VS0_EN	63 73
1A	PM	P5VS3_EN	63 70
1A	PM	PCHCORE_REG_EN	63 69
1A	PM	PCHCORE_REG_PG00D	63 64 69
1A	PM	PEG RESET L	8 27
1A	PM	SDCARD_RESET	20 44 92

NET_TYPE			
PHYSICAL	SPACING		
1A	PM	4V5_REG_EN	56
1A	PM	ALL_SYS_PWRGD_R	5 64
1A	PM	ALL_SYS_PWRGD_SMC	46 64
1A	PM	CK505_27MHZ_EN	25
1A	PM	CPUVTT_REG_EN	63 68
1A	PM_VTT	CPUVTT_REG_PG00D	10 63 64 68
1A	PM	CPU_MEM_RESET L	10 26
1A	PM	DDRVT EN	63 71
1A	PM	DEBUG_RESET L	27 48
1A	PM	FWPHY_RESET L	39
1A	PM	FWXIO_SNOOP_EN	39
1A	PM	FW_RESET L	27 39
1A	PM	ENET_RESET L	27 37
1A	PM	MEM_RESET L	26 30 31
1A	PM	MINI_RESET L	27 33
1A	PM	SMC_DELAYED_PWRGD	47 64
1A	PM	SMC_LRESET L	27 46
1A	PM	SMC_RESET L	46 47 48
1A	PM_VTT	XDP_CPUPWRGD	10 24
1A	PM_VTT	XDP_DBRESET L	10 24 27
1A	PM_VTT	XDP_PWRGD	24



J4700 USB CAMERA

89 5

IN

PP5V_S3

MIN_ALLOWED_TPS=1

FUNC_TEST=TRUE

85 44

IN

USB_CAMERA_L_P

FUNC_TEST=TRUE

85 44

IN

USB_CAMERA_L_N

FUNC_TEST=TRUE

85 44

IN

USB_BT_L_P

FUNC_TEST=TRUE

85 44

IN

USB_BT_L_N

FUNC_TEST=TRUE

49 44

IN

=SMB_ALS_SCL

FUNC_TEST=TRUE

49 44

IN

=SMB_ALS_SDA

FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700

1 PP3V3_S3 TESTPOINT NEAR J4700

6 GROUND TESTPOINTS NEAR J4700

J4750 USB CARD READER

85 44

IN

USB_SDCARD_L_P

FUNC_TEST=TRUE

85 44

IN

USB_SDCARD_L_N

FUNC_TEST=TRUE

91 44 20

IN

SDCARD_RESET

FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750

2 Ground Testpoints near J4750

J4780 IR BOARD

85 44

IN

USB_IR_L_P

FUNC_TEST=TRUE

85 44

IN

USB_IR_L_N

FUNC_TEST=TRUE

89 44

IN

PP5V_S3_IR_FLT

FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J4780

J4520 SATA ODD (HIGH SPEED)

46 42

IN

SMC_ODD_DETECT

FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520

1 GROUND TESTPOINTS NEAR J4520

J5551 ODD TEMP SENSOR

88 52

IN

SNS_ODD_P

FUNC_TEST=TRUE

88 52

IN

SNS_ODD_N

FUNC_TEST=TRUE

J5600 ODD FAN

53

IN

FAN_0_PWR_L

FUNC_TEST=TRUE

53

IN

FAN_TACH0_L

FUNC_TEST=TRUE

89 53

IN

PP12V_S0_FAN0_L

FUNC_TEST=TRUE

53

IN

FAN_0_GND

FUNC_TEST=TRUE

J5700 CPU FAN

54

IN

FAN_2_PWR_L

FUNC_TEST=TRUE

54

IN

FAN_TACH2_L

FUNC_TEST=TRUE

89 54

IN

PP12V_S0_FAN2_L

FUNC_TEST=TRUE

54

IN

FAN_2_GND

FUNC_TEST=TRUE

88 54 52

IN

SNS_AMB_P

FUNC_TEST=TRUE

88 54 52

IN

SNS_AMB_N

FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J5700

J5601 HD FAN

53

IN

FAN_1_PWR_L

FUNC_TEST=TRUE

53

IN

FAN_TACH1_L

FUNC_TEST=TRUE

89 53

IN

PP12V_S0_FAN1_L

FUNC_TEST=TRUE

53

IN

FAN_1_GND

FUNC_TEST=TRUE

J5400 HDD TEMP SENSOR

88 51

IN

HDD_OOB_TEMP_FILT

FUNC_TEST=TRUE

1 GROUND TESTPOINTS NEAR J5400

J5560 SKIN TEMP SENSOR

88 52

IN

SNS_SKIN_P

FUNC_TEST=TRUE

88 52

IN

SNS_SKIN_N

FUNC_TEST=TRUE

J6601 AUDIO MICROPHONE

60

IN

AUD_MIC_IN1_N_CONN

FUNC_TEST=TRUE

60

IN

GND_AUDIO_MIC1_CONN

FUNC_TEST=TRUE

60

IN

AUD_MIC_IN1_P_CONN

FUNC_TEST=TRUE

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

85 60 58

IN

AUD_SPKR_OUTL02R_POUT

FUNC_TEST=TRUE

85 60 58

IN

AUD_SPKR_OUTL02R_NOUT

FUNC_TEST=TRUE

85 60 58

IN

AUD_SPKR_OUTL01R_POUT

FUNC_TEST=TRUE

85 60 58

IN

AUD_SPKR_OUTL01R_NOUT

FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

85 60 58

IN

AUD_SPKR_OUTL02L_POUT

FUNC_TEST=TRUE

85 60 58

IN

AUD_SPKR_OUTL02L_NOUT

FUNC_TEST=TRUE

85 60 58

IN

AUD_SPKR_OUTL01L_POUT

FUNC_TEST=TRUE

85 60 58

IN

AUD_SPKR_OUTL01L_NOUT

FUNC_TEST=TRUE

J6600 AUDIO AUXILIARY CONNECTOR

89 60

IN

PP3V3_AUDIO_SPDIF JACK

MIN_ALLOWED_TPS=2

FUNC_TEST=TRUE

60

IN

AUD_LI_DET JACK

FUNC_TEST=TRUE

60

IN

AUD_LI_R JACK

FUNC_TEST=TRUE

60

IN

AUD_LI_GND JACK

FUNC_TEST=TRUE

60

IN

AUD_LI_L JACK

FUNC_TEST=TRUE

60

IN

HS_MIC_LO JACK

FUNC_TEST=TRUE

60

IN

HS_MIC_HI JACK

FUNC_TEST=TRUE

60

IN

AUD_HP_L JACK

FUNC_TEST=TRUE

60

IN

AUD_HP_GND JACK

FUNC_TEST=TRUE

60

IN

AUD_HP_R JACK

FUNC_TEST=TRUE

60

IN

AUD_HP_TYPERDET JACK

FUNC_TEST=TRUE

60

IN

AUD_IP_PERPH JACK

FUNC_TEST=TRUE

60

IN

AUD_HP_TIPDET JACK

FUNC_TEST=TRUE

60

IN

AUD_SPDIFIN JACK

FUNC_TEST=TRUE

60

IN

AUD_SPDIF_OUT JACK

FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J6600